Electrodeposited Platinum Electrode for FeRAM

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Introduction

The purpose of this study is to prepare the electrodeposited Platinum(Pt) electrode, which is used for the lower electrode of FeRAM (Ferroelectric Random Access Memory). The optimum Pt electrodeposits have been examined by structural analysis and electrometric measurement of the electrodeposits. We further discussed the effect of hydrogen during the annealing of Pt electrodeposits.

Experimental

The silicon wafer surface consists of Ti adhesive layer and Pt seed layer. The lower electrode was electrodeposited on this Pt seed layer. The Pt electrodeposits were annealed in order to improve the crystalline orientation. This Pt electrodeposited layer with annealing acts as the lower electrode for capacitor. Then PZT (Piezo Material Lead Zirconate Titanate) layer was formed on the lower electrode by MOCVD (Metal-Organic Chemical Vapor Deposition). Upper Pt patterned layer was formed by sputtering with lift off process.

The surface morphology of the deposits was observed by FE-SEM. The structure of the Pt electrodeposition layer and Pt seed layer was identified by X-ray diffraction analysis. The concentration profile of each element in the metal layer was measured by GDS (Glow Discharge Spectroscopy). Electrical properties were measured by a low frequency impedance analyzer, an electrometer, Sawyer-Tower circuit, a pulse generator and a digitizing oscilloscope.

Results and Discussion

1) The Pt lower electrode was formed on the Ti seed layer. Both 5nm and 15nm thickness of Ti seed layer were used. The maximum degree of crystalline orientation of Pt electrodeposits was observed with annealing at 773 K for 1 hour for 5nm Ti seed layer thickness. With 5nm Ti seed layer thickness, the degree of crystalline orientations are far much better than 15nm thickness.

2) Pt-PZT-Pt capacitor was prepared by the formation of Pt upper electrode by Pt-sputtering/lift off after forming CVD PZT layer on the Pt electrodeposits. From the D-V characteristic of Pt-PZT-Pt capacitor (Fig. 1-a), well-saturated D-E hysterisis loop was obtained with the Ti seed layer thickness of 5 nm. Pt-PZT-Pt capacitor of Ti seed layer thickness of 15 nm barely showed ferroelectric D-E hysterisis loop. I-V characteristics of Pt-Pt capacitors are shown in Fig. 1-b. The current density in both positive and negative bias regions increased with 15nm thickness of Ti seed layer.

3) SEM image of annealed Pt electrodeposits with Ti seed layer thickness of 15nm shows numerous holes due to H_2 gas formation(Fig.2). While, almost no holes were observed on the Pt electrodeposits with Ti seed layer thickness of 5nm. From GDS measurement, hydrogen profile shows maximum at the Ti sputtering seed layer.

Reference

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2)M.Shimizu : Proceedings of the 2000 12th IEEE International Symposium on Applications of Ferroelectrics(2000) pp.961-964

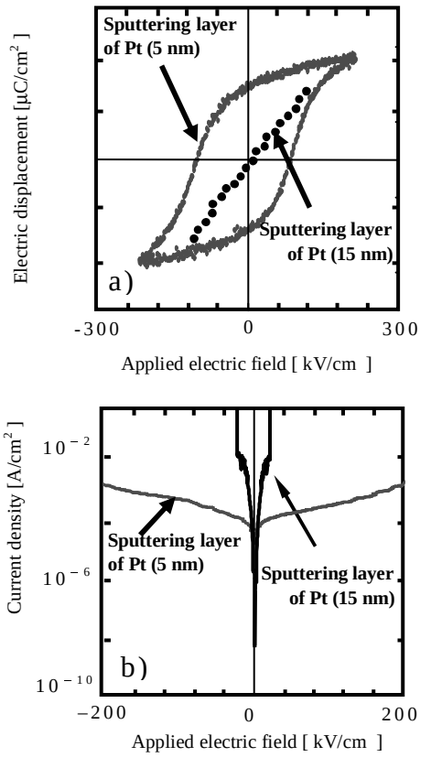

Fig. 1 Electric characteristic of Pt capacitor
(a) D-V characteristic of capacitor
(b) I-V characteristic of capacitor

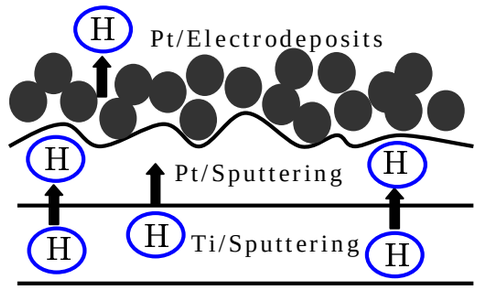

Fig.2 Degregation mechanism of F electrodeposits cristailline orientation.