Practical Considerations from Simulation of Damascene Copper Plating

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There has been much recent progress in numerical simulation of Damascene copper plating.[1-8] Although detailed mechanistic descriptions of the superconformal growth mechanism continue to be debated, our focus is on deriving practical utility and insight from available models, even as they continue to be revised and corrected. We concentrate on the widely recognized curvature-enhanced-accelerator-coverage (CEAC) model,[2,3] but also on variations of this model that incorporate additional elements, some empirical and others hypothetical. We consider shape evolution in the context of industrially relevant cavity profiles, and we examine the limits of void-free cavity filling with reference to the shapes and locations of voids observed in practical vias and trenches. We also look at the applicability of feature-fill models to estimates of the extent of overplating[9] above densely trenched regions.

References

1. A.C. West, S. Mayer, and J. Reid, *Electrochem. Solid State Lett.*, **4** (7) C50-C53 (2001).
2. T.P. Moffat, D. Wheeler, W.H. Huber, and D. Josell, *Electrochem. Solid-State Lett.* **4** (4) C26-C29 (2001).
3. K. Josell, D. Wheeler, W.H. Huber, and T.P. Moffat, *Phys. Rev. Lett.*, **87**, 016102 (2001).
4. D. Josell, D. Wheeler, W.H. Huber, J.E. Bonevich, and T.P. Moffat, *J. Electrochem. Soc*, **148** (12) C767-C773 (2001).
5. D. Josell, D. Wheeler, and T.P. Moffat, *Electrochem. Solid-State Lett.* **5** (4) C49-C52 (2002).
6. D. Wheeler, D. Josell, and T.P. Moffat, *J. Electrochem. Soc*, **150** (5) C302-C310 (2003).
7. T.J. Pricer, M.J. Kushner, and R.C. Alkire, *J. Electrochem. Soc*, **149** (8) C406-C412 (2002).
8. U. Landau, E. Malyshev, R. Akolkar, and S. Chivilikhin, Conference Proceedings, "Electrodeposition Processes in Semiconductor Device Fabrication," AIChE Annual Meeting, 2003, Paper 189d, pp. 22-35
9. C. Yu and J.O. Dukovic, Abstract 168 from ECS 205th Meeting (2004) and ECS Proceedings Volume "Electrochemical Processing in ULSI and MEMS," H. Deligianni, S.T. Mayer, T.P. Moffat, G.R. Stafford, eds. (2004) (forthcoming).