Wafer-scale Current and Potential Transients during Copper Metallization of Semiconductor Interconnects

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The damascene process for copper metallization of interconnects on semiconductor wafers[1] has become the mainstay technology for manufacturing advanced semiconductor devices. Fundamental understanding and quantitative modeling of the process, however, has lagged behind its practical implementation. A number of models, based on quite different assumed mechanisms and thus leading to different conclusions have been proposed[1-7]. Furthermore, just about all via-scale models have focused on the deposit build-up in a single via and have not linked the analysis to wafer-scale operating conditions. It is well recognized that global process parameters, e.g., current and voltage waveforms have critical effect on obtaining defect-free feature-fill. In order to optimize the operating conditions for the feature-scale parameters, models on the two scales must be coupled.

Recently, Akolkar and Landau[5-7] have shown that the time-dependent interactions due to the vastly different diffusion and adsorption constants of the plating additives used in wafer metallization, provide the essential conditions for a defect-free bottom-up fill. According to this transient-diffusion-kinetics ('TDK') model, the plating inhibitor polyethylene glycol ('PEG'), is transport limited and requires a few seconds to reach the via bottom. This time delay enables the faster diffusing Bis(3-sulfopropyl)-disodium sulfonate ('SPS'), to adsorb at the via bottom, blocking further PEG adsorption at this site, and thus promoting a rapid bottom-up growth. Transport limitations are minimal at the wafer surface, enabling the faster adsorbing PEG to inhibit this region. The stronger adsorbing SPS eventually displaces the PEG from the wafer surface, leading to a delayed enhancement of plating at the surface.

Here, we couple the single-via TDK model to wafer-scale process simulations[8] to provide the essential link between the nano-scale feature parameters and macroscopic process conditions. Wafer-scale parameters such as the via loading, wafer potential and total current, flow (due to wafer rotation and impinging flow), wafer size (200 vs. 300 mm), and the electrolyte composition (i.e., additives concentrations) are considered. Location-dependent and time-dependent current densities are obtained from the transport-kinetics equations. Summation of the area-weighted local current densities provides the total wafer current (Fig.1). Implications of the additives transport-kinetics processes to the wafer scale metallization is discussed and guidelines for optimal selection of process parameters are presented.

References

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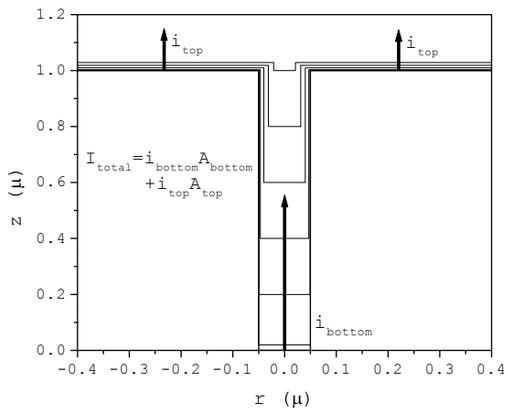

Figure 1. Schematic showing the growth profiles during the 'bottom-up' fill in a via with R=0.05 μ and depth=1 μ. The current density at the via bottom is significantly larger than that at the wafer top surface ($i_{bottom} >> i_{top}$). These local current densities, however, are strongly time-dependent due to the unsteady state interactions between the additives species that affect the local kinetics. The total wafer current, which is the summation of the area-weighted local current densities, is therefore a function of time. All dimensions are in microns.