Magnetic Tunnel Junction-Based MRAM and Related Processing Issues

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Interest in spin-electronics has surged over the past 6 - 8 years. Magnetic tunnel junctions (MTJ) (1) are an important subset of this field. They are showing increasing attractiveness for use in high-speed, non-volatile, magnetic random access memory (MRAM).

In a typical MTJ stack, an antiferromagnetic (AF) layer, e.g. a Pt-Mn alloy, is located above the bottom electrode. This pins the lower ferromagnetic (FM) layer of an antiparallel (AP), Ru-coupled FM sandwich. A thin (10 – 20Å) AlO_x barrier layer separates the FM free layer on top from the AP-pinned sandwich layers. The tunneling current (part of which is spin polarized) depends on the relative orientation of the magnetizations of the two FM layers, which can be changed by an applied magnetic field. The junction resistance, which is often called tunneling magnetoresistance (TMR), is lowest when the moments of the FM layers are parallel. Currently, disclosed values of TMR measured at room temperature range as high as 70 % (2, 3).

A "half-select" process, in which a pair of orthogonal lines each provide half of the switching field to change magnetization direction of the free layer, has been the standard MTJ switching method. This method can give rise to inadvertent writing of bits, which has stimulated investigation of improved writing methods with wider margins. The foremost of these is the "toggle" method (4, 5). This utilizes a multi-film free layer structure, with an FM layer above and below a conducting spacer layer. The field-generating lines are at 45° to the magnetization of the bits, drastically reducing the chances of switching a non-selected bit.

A number of companies have announced demonstrator MRAM chips. The current trend seems to be towards rapid development of chips with high writing endurance in the range 1 - 16 Mbit size for potential use in niche applications. Motorola's 4Mb chip (4, 6) uses the new toggling writing scheme. It is based on a 5-level-metal, 0.18 µm CMOS technology with a bit cell size of 1.5µm^2. IBM and Infineon have jointly developed a high-speed 128 Kbit MRAM core (7) and are fabricating a 16Mb MRAM chip (8). The latter is based on 0.18 µm, three-level-Cu CMOS, and has a three-level MRAM structure and a 1.42 µm^2 bit cell.

MTJ Processing Issues

The impressive gains made in MTJ performance in the past few years, particularly in TMR, have been in large part fueled by materials research. The fabrication of durable, high-yield MTJ arrays, which use the advances in materials, poses major processing challenges, however.

Following preparation of a smooth surface (a few Å RMS of roughness) by, e.g. CMP, stack films are usually deposited using PVD or IBD methods. A damage-free plasma process may be used to oxidize a 6 – 12 Å Al layer to form the tunnel barrier. It is critical that the barrier be pinhole free, and that the pinned FM layer not become oxidized. Annealing tends to be a critical step in reaching high TMR values; e.g., Han et al. (9) observed that TMR increased from 22 % to 50 % on annealing MTJs (large area) at 300 °C.

In contrast to Cu interconnects, MTJs tend to be fabricated using stack etching-based processes rather than Damascene-based processes. Re-deposition of metal during etching (ion milling or RIE) may create deleterious fences on sidewalls resulting in shorting. MTJ stack etches ideally should be followed by a rinse to reduce the extent of such fences. Due to the possibility of Galvanic corrosion, this method, if improperly carried out, is fraught with difficulty. Song et al. (10) recently reported that MTJs with Ir-Mn AF layers showed degraded properties when dilute HCl and HNO_3 acid treatments were used after ion mill patterning; selective etching, e.g. of Mn, was severe at the Ir-Mn/Co-Fe interface.

Much attention has been paid to the thermal stability of MTJs (11) due to the desire to integrate MTJs with standard back end of line (BEOL) CMOS processing. Diffusion of Mn from the AF layer and FM layer/barrier interface degradation at elevated temperatures, for instance, have been a concern of several groups. A number of methods have been explored to address these problems. Batlle et al. (11) took the novel step of inserting a partially oxidized Fe layer between the pinned Co-Fe alloy layer and the AlO_x barrier. They observed TMR values of up to 39% following annealing at 380 – 390 °C, although MR decreased on annealing at intermediate temperatures. From a CMOS integration point of view, control of junction resistance spreads, rather than maintenance of initially high TMR, is likely to be a more critical processing issue.

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