High Breakdown Field (> 15MV/cm) on Crystalline □-Ga_2O_3/GaN Metal Oxide Semiconductor Devices

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We investigate the crystallinity effect of gallium oxide (Ga_2O_3) on the electrical properties of n-gallium nitride (GaN) metal oxide semiconductor (MOS) devices. Shown in Fig.1, the x-ray diffraction analyses of the oxide layer identified the signals from the (019) and (024) planes of monoclinic phase □-Ga_2O_3, indicating the crystallinity of Ga_2O_3 layer. A thin strain-relieving layer (~ 20nm) of gallium oxynitride (GaON) with graded composition[1], as revealed by the x-ray photoemission spectroscopy, is shown to assist the oxide growth on GaN in the photo-electro-chemical process[2]. Standard MOS structure with crystalline □-Ga_2O_3 layer on GaN was fabricated through lithography process. In Fig.2, improved MOS characteristics with high forward breakdown field E_{FB} > 15 MV/cm, and high value of gate oxide barrier height □$_B$ ~ 2.2 eV were observed. In Fig.3, a narrow hysteresis width of 0.26V, fixed oxide charge density N_f ~ 8.6×10^{10} cm^{-2} and a flat band voltage of ~ 1.42V and outstanding low interface state density D_{it}~ 3.5×10^{11} cm^{-2}-eV^{-1} extracted by the conductance method were observed[3]. These observations are ascribed to the formation of crystalline Ga_2O_3 layer as the oxide is transformed from a hydrous status into a monoclinic phase during a post-growth thermal annealing in O_2 ambience.

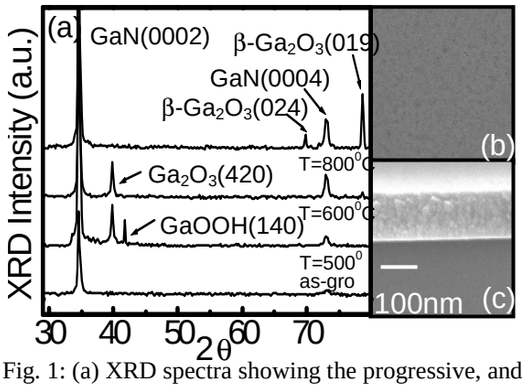

Fig. 1: (a) XRD spectra showing the progressive, and SEM micrograph showing (b) planar and (c) cross-section view of a Ga_2O_3 layer with ~150nm thickness on GaN.

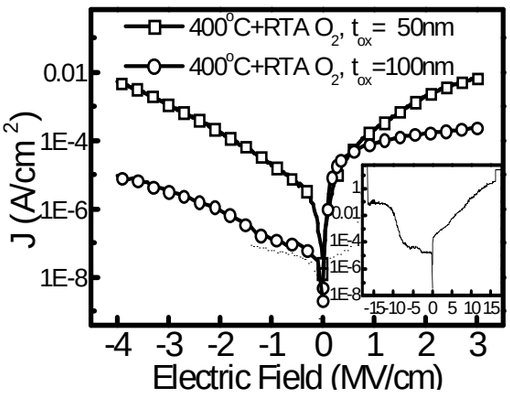

Fig.2: Gate leakage current density on electric field in Ga_2O_3/GaN MOS devices with 50 and 100nm oxide thickness. Inset: showing a forward breakdown occurred at 15 MV/cm for the 50nm-thick Ga_2O_3/GaN MOS.

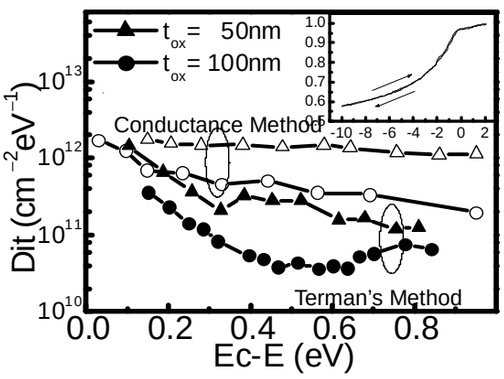

Fig. 3: Measured interface state density for the 50nm and 100nm –thick Ga_2O_3/GaN MOS devices by the Terman and conductance methods, respectively. Inset: showing a narrow hysteresis window (~ 0.26V)

Reference

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3. B. Gaffey, L. J. Guido, X. W. Wang, and T. P. Ma, IEEE Trans. Electron Dev. 48, 458 (2001)