Abs. 1289, 206th Meeting, © 2004 The Electrochemical Society, Inc.

Strained-Si/SiGe-On-Insulator CMOS technology as a platform of device performance boosters

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MOSFETs with a high mobility channel are currently stirring a strong interest as advanced CMOS device structures, which can relax several physical limitations associated with device scaling. From this viewpoint, MOSFETs with strained-Si/relaxed SiGe structures are promising for high performance/low power CMOS applications, because of the high electron and hole mobility. However, it has been recognized that there exist several problems to be overcome in realizing strained-Si CMOS LSI, inherent to strained-Si channels. On the other hand, strained-Si/SiGe-On-Insulator (strained-SOI) MOSFETs, where high mobility channel is combined with SOI structures, are expected to mitigate these problems. Furthermore, strained-Si/SiGe-On-Insulator structures allow us to provide a wide range of new device options, including or integrating a variety of technology boosters and technology flavors. This paper presents our recent results on the device design and the fabrication of strained-SOI CMOS and a future possible direction of channel engineering using strained-Si/SiGe-On-Insulator structures.

As one of the optimum device structures for high device performance, we have proposed and demonstrated strained-SOI MOSFETs[1]-[3]. The experimental enhancement factors of electron and hole mobility, which amount roughly to twice, are almost the same between bulk strained-Si and strained-SOI channels. It has also been shown that the strained-SOI structure enables to suppress floating body effects, attributable to larger hole current flow through SiGe pn- junction in the source.

Furthermore, fully-depleted (FD) strained-SOI MOSFETs having a ultra-thin body and low impurity concentration become more attractive, because of (1) maximized mobility due to low impurity scattering and low E_{eff}, (2) suppression of short channel effects (3) low junction capacitance and low leakage current and (4) reduction in statistical variation of V_{th}.

The most important fabrication process of strained-SOI CMOS is the preparation of thin and relaxed SGOI substrates with minimal dislocation density. We have successfully fabricated these SGOI substrates by using our original approach, called the Ge condensation process[1],[4],[5]. The main process consists in the oxidation of SiGe/SOI structures. The rejection of Ge atoms from thermal oxide, the block of Ge diffusion toward Si substrates by buried oxides and the relaxation of SiGe films through the existence of SiGe/buried oxide interface are key issues. Since this process is based on epitaxial growth and oxidation, superior uniformity of film thickness and Ge content, and the applicability to extremely-thin strained-SOI films with high Ge content are expected. Fig. 1 shows the photo of a 200 nm strained-SOI substrates with effective Ge content of 21 % and the strain variation over a wafer. A fairly uniform strain profile is confirmed.

It has been demonstrated that strained-SOI CMOS 101-stage CMOS ring oscillators exhibited 70 - 30 % faster switching speed than conventional SOI CMOS[6].

Possible directions of channel engineering at present and in the future are summarized in Fig. 2.Two different directions of channel structure engineering, high mobility new channel materials and 3D channel structures could be merged in the future, because of strong requirement of both current drive and SCE suppression. We have successfully fabricated a strained-Si-On-Nothing (SSON) structure[7], which is one possible building block of double gate strained-Si CMOS, by etching only SiGe under the channel region on strained-SOI substrates.

Another direction regarding new channel materials is Ge MOS and ultra-thin Ge-On-Insulator (GOI) MOS structures. We have recently succeeded in fabricating ultrathin GOI substrates (7 nm, Ge content higher than 99.9 %) by the Ge condensation technique[8], shown in Fig. 3. It has been confirmed that the GOI thickness can be controlled from 2 nm to 25 nm by changing the total amount of Ge before the condensation.

In summary, it is strongly expected that MOSFETs based on Si/SiGe hetero-structures can provide new device options to sub-100 nm CMOS technology with high performance/low power consumption.

The authors would like to thank M. Hirose, T. Kanayama, S. Kawamura and T. Masuhara for their continuous supports. This work was supported by NEDO.

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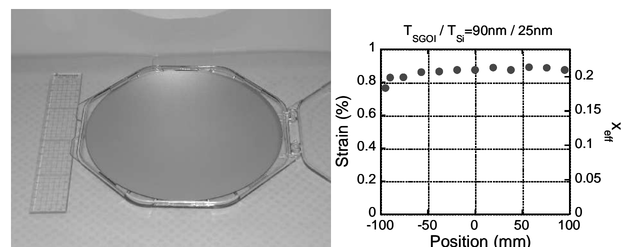

Fig.1 200 mm strained-SOI wafers and the uniformity of strain over a whole wafer.

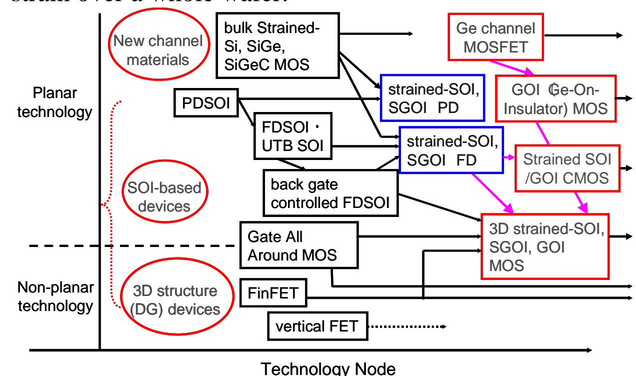

Fig. 2 Future possible directions of channel engineering

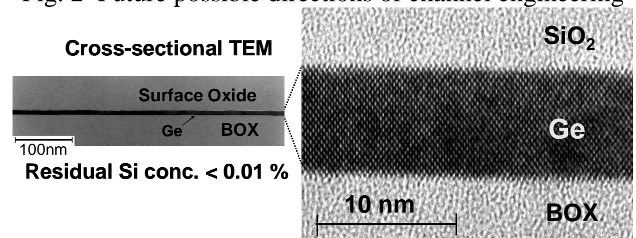

Fig. 3 Cross-sectional TEM image of fabricated Ge-On-Insulator (GOI) structures with Ge thickness of 7 nm.