

Application of selective SiGe epitaxy for recessed source/drain of PMOS transistor

Yihwan Kim, Arkadii Samoilov, Lori Washington,
Andrew Lam, Nick Dalida, Mark Kawaguchi, and Meihua
Shen
Applied Materials
974 E. Arques, Sunnyvale, CA 94086, USA

Use of SiGe in recessed source/drain areas (S/D) of a PMOS transistor gives two important benefits in terms of transistor performance improvement. One comes because SiGe, due to a different lattice constant than that of Si, induces strain in the channel of the device, which can be used to improve mobility of the charge carriers (1). The other benefit is from a decrease of the source/drain electrical resistance and abrupt junction formation. SiGe incorporates more dopants than Si and reduces source/drain resistance. Boron diffusion in SiGe is retarded compared to diffusion in Si (2, 3). Also, SiGe has a smaller band gap than that of Si and, consequently, a reduced barrier height between metal and semiconductor, which results in a lower contact resistance (4).

We have investigated the application of selective SiGe epitaxy for recessed S/D of a PMOS transistor. Not only the selective epitaxy process of heavily boron doped $\text{Si}_{1-x}\text{Ge}_x$ ($X=0.15\sim 0.3$) but also the recessed area formation by Si etch and post-etch cleaning have been developed. Selective SiGe epilayer was deposited by reduced pressure thermal chemical vapor deposition (RPCVD) in an Epi Centura. In-situ boron doped SiGe epilayer shows junction abruptness of < 3 nm/decade, near 100% dopant activation without a subsequent heat treatment, and resistivity of $< 0.001 \Omega \text{ cm}$, which will satisfy source/drain extension requirements of 65 nm or smaller technology node according to the ITRS roadmap. Details can be found elsewhere (3). Fig. 1 shows the boron doped selective SiGe epilayer grown on recessed source/drain of PMOS transistor. 100% selectivity and smooth film morphology was observed.

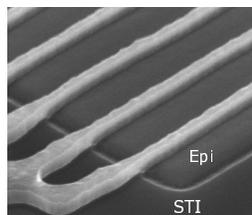


Fig. 1. Top view scanning electron microscopy image of a transistor with boron doped selective SiGe epilayer grown on recessed source/drain.

We will discuss two integration schemes to incorporate selective SiGe epitaxy into the transistor fabrication. One scheme is recess formation and selective SiGe epitaxy before spacer sidewall formation and deep source/drain implantation (pre-spacer epi process). In this case, the compressively strained SiGe epilayers that fill the recessed S/D are very close to each other, efficiently straining the channel region. The other scheme is post-spacer epitaxy, that is, the epitaxy after spacer sidewall formation. In this case, the epilayer can be pulled in closer to the channel with a use of isotropic Si etch to make an undercut underneath the spacer during the recess formation. We have developed two types of Si etch profiles: vertical etch and isotropic etch, as shown in Fig. 2. Depending on the recess profile, the stress induced in the channel by the strained SiGe epilayer will be changed. The value of stress in the channel with different recess profiles and Ge concentration can be estimated by computer simulation. Fig. 3 shows simulation result. It was done for SiGe epitaxy with 25% of Ge concentration,

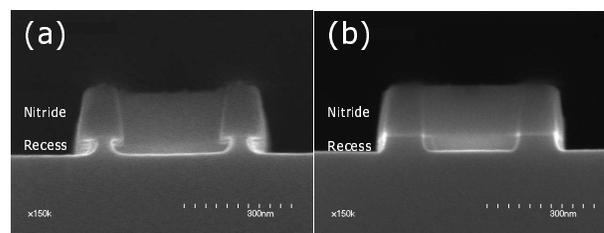


Fig. 2. Cross sectional scanning electron microscopic images of recessed area by Si etch. (a) isotropic etched profile and (b) vertical etched profile.

which is corresponding to 1.8 GPa compressive stress in the epilayer. The epilayer filled 75 nm deep recessed source/drain areas. Fig. 3(a) shows two-dimensional distribution of stress. Due to the compressively strained SiGe epilayer, the channel area is also strained compressively while the Si area below the SiGe epilayer shows tensile stress. A graph of stress value as a function of the distance from the SiGe/Si interface along the gate length direction is shown in Fig. 3(b). The horizontal line cut of the two-dimensional data is 20 nm from the Si surface. The value of stress along the channel decreases with the distance from the SiGe/Si interface. Stress in the channel is affected by a function of the Ge concentration in the SiGe epilayer and the recess depth. The computer simulations are thus helpful to achieve a desired value of stress in the channel and optimized device performance.

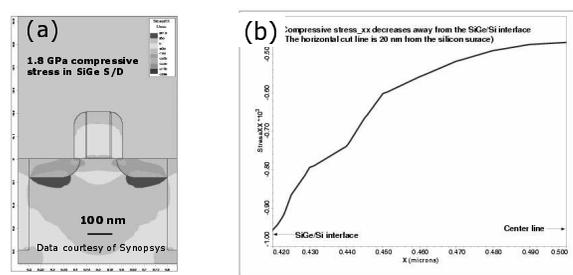


Fig. 3. Simulation results of stress induced by strained SiGe epitaxy on recessed source/drain area. (a) two-dimensional distribution of stress and (b) stress as a function of distance from the SiGe/Si interface along the channel.

In addition, we will present results of a study of effects of implantation and subsequent thermal annealing on properties of the SiGe epilayer by secondary ion mass spectroscopy and x-ray diffractometer. Implantation of boron has been done with different energy and dose into both undoped and doped SiGe epilayers.

To summarize, we have developed a selective epitaxy and Si etch process flow, in which the stress in the channel can be optimized by computer simulations.

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