Epitaxially Strained SiGe Process to Improve Mobility in the PMOS Transistor

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A novel approach to introduce compressive stress in the PMOS channel by a strained SiGe layer incorporation at the drain extension (DE) location is discussed. Previously, epitaxial SiGe grown in a recessed source/drain (SD) has been used to improve hole mobility [1]. Epitaxial SiGe growth and integration at the DE location has many advantages. The stress from SiGe layer monotonically decays as a function of distance, therefore when SiGe is present at close proximity to the channel the magnitude of compressive stress transfer is higher. Since Boron can be activated to a higher concentration in the SiGe layer compared to bulk silicon, the net extension resistance will be lower. The surface of silicon at DE locations is cleaner and more conducive to epi-growth; also, the additional thermal budget from epi-clean and deposition is less of a concern at the DE location. Fig 1 shows a TEM cross-section of the state of the art 37 nm gate length PMOS devices with the epitaxial SiGe layer incorporated at the DE location.

A 35% improvement in the transistor drive current is observed from this device compared to the reference device with no SiGe. Figure 2 illustrates this result as an improvement in the on-state drive current compared to the off-state current. Detailed simulations and additional TEM characterization will be used to quantitatively isolate the improvements from stress and resistance improvements.

References:

[1] T. Ghani et. al. IEDM Digest 2003 p. 978.

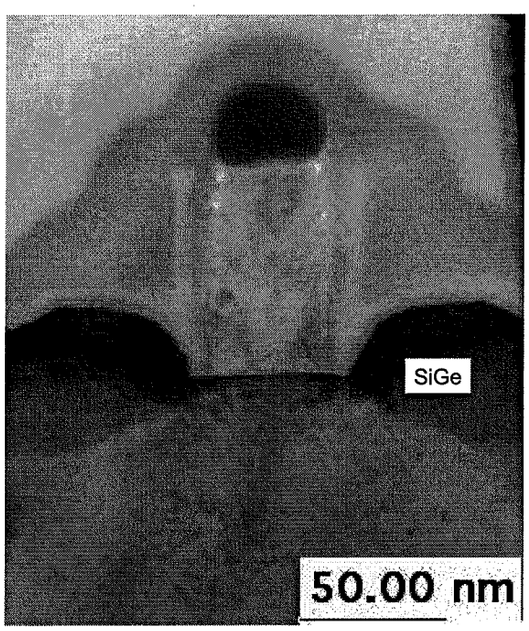

Fig 1. TEM cross-section of 37 nm gate with SiGe layer in the DE region

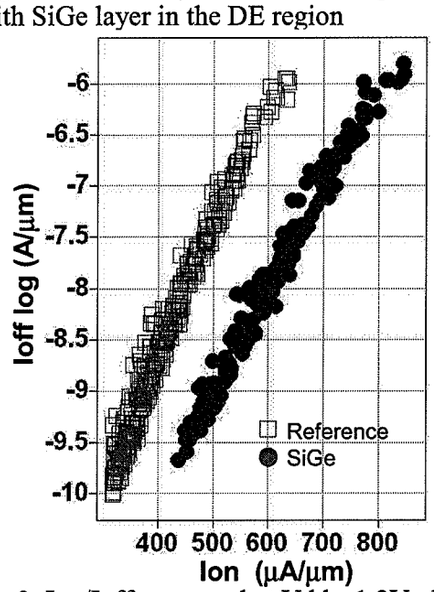

Fig 2. Ion/Ioff measured at Vdd=-1.2V plot showing the improvement with SiGe layer