Integration issues of a new method for formation of shallow junctions in MOSFET structures using recessed and selectively regrown $Si_{1-x}Ge_x$

C. Isheden, H. H. Radamson, P.-E. Hellström, and M. Östling

KTH (Royal Institute of Technology), Department of Microelectronics and Information Technology, P.O. Box Electrum 229, SE-164 40 Kista, Sweden.
Phone: +46 8 7904328 Fax: +46 8 7527850
*E-mail: isheden@imit.kth.se

ABSTRACT

MOSFET device scaling according to the ITRS roadmap requires continuous reduction of the parasitic resistances. To obtain this, shallow source/drain (S/D) junctions with high active doping concentration are needed. Conventional ion implantation reaches its limit when resistivities corresponding to doping levels above the solid solubility in Si are required. Therefore novel techniques have to be innovated to maintain the rate of development in device technology. A new approach has been proposed for creating shallow junctions using a Si etch step followed by selective epitaxial growth (SEG) of high boron doped $Si_{1-x}Ge_x$ layers [1]. The method has been developed further by performing the Si etching step (using HCl) and the SEG in the same run in a reduced pressure CVD reactor [2-3]. This is an attractive method since no wafer cleaning is needed before the epitaxial growth, which would have a detrimental effect on the sensitive thin gate oxide. In the process, the crystalline quality of the $Si_{1-x}Ge_x$ layers and the electrical characteristics of the junctions are affected by the surface quality of the patterned substrate. The oxide spacers are dry-etched using reactive ion etching (RIE), which is known to create defects on the Si surface. In the subsequent HCl etching step, a damaged Si surface results in a low-quality Si surface, which degrades the epitaxial quality of $Si_{1-x}Ge_x$. As a consequence, the resistivity and surface roughness of the layers are significantly increased.

In this paper, a series of different ways of opening the oxide using RIE were examined in order to improve the layer quality. The results showed that opening the oxide with a two-step process using CHF_3/O_2 in the first step and NF_3 in the second step is successful for obtaining a high-quality Si surface after the RIE step. This is illustrated in Fig. 1. There is some nucleation on the oxide surface in figure 1a indicating a degrading of selectivity during the epitaxial growth. It is believed that this is due to the RLE damages on SiO_2. Applying an appropriate recipe in RLE step has solved these problems. In this way, the I-V characteristics of PMOSFETs using recessed highly B-doped $Si_{1-x}Ge_x$ junctions have been improved.

Process control issues have been also discussed in these investigations. The pattern dependencies during the etching or epitaxy were calibrated by atomic force microscope and focussed x-ray beam.

.

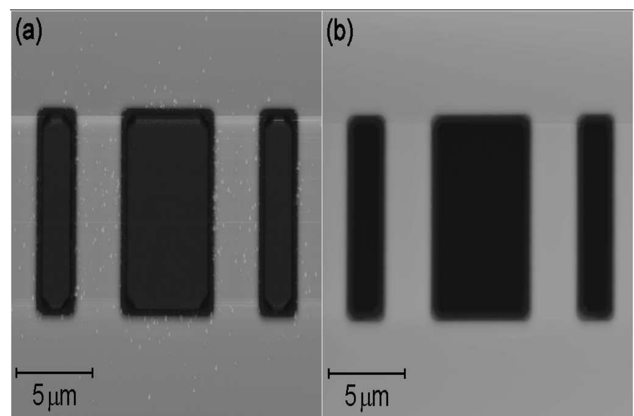

Fig. 1. AFM pictures of SiGe surfaces grown selectively (after HCl etching) on the substrates processed by (a) CHF_3/O_2 and (b) CHF_3/O_2 followed by NF_3 in the RIE chamber. The surface quality and layer roughness are significantly improved in (b).

REFERENCES

[1] S. Gannavaram, N. Pesovic and M. C. Özturk, IEDM Tech. Digest, 437 (2000).

[2] C. Isheden, P.-E. Hellström, H. H. Radamson, S.-L. Zhang and M. Östling, in press in Electrochem. Solid-State Lett.

[3] R. Loo, M. Caymax, P. Meunier-Beillard, I. Peytier, F. Holsteyns, S. Kubicek, P. Verheyen, R. Lindsay and O. Richard, Appl. Surf. Sci. **224**, 63 (2004).