Strain Relaxation in Narrow Width Strained Silicon Devices with Poly and Metal Gates

Z. Krivokapic, V. Moroz*, L. Smith*, Q. Xiang, M.R.Lin
AMD, Technology Research Group, M/S 143, Sunnyvale, CA 94088-3453, USA
* Synopsys, 700 East Middlefield Road, Mountain View, CA 94043, USA
e-mail: zoran.krivokapic@amd.com

The scalability of strained silicon is an important issue for sub-65nm technology node. While it has been reported that performance enhancement diminishes with smaller channel length [1,2], the impact of channel width has not been reported yet. In this paper we present experimental data for 35nm long gates with different channel width, using unstrained and strained (20% germanium content) bulk wafers. Furthermore, we show the impact of metal gate (FUSI NiSi gate) on channel strain management. Since it is extremely difficult to extract mobility from 35nm long devices with very small channel width we compared linear transconductance of strained and unstrained devices for both poly and FUSI gates. The first observation is that trend of enhancement by the strained silicon layer changes with the choice of gate material. For NMOS devices with poly gate enhancement increases with narrower gates, while for FUSI gates it starts to decrease (Fig. 1). For PMOS devices and our particular germanium content we see degradation by using strained silicon layer. This degradation becomes worse with narrower gates and it is more pronounced for FUSI gates. We verify our experimental data with 3-d computer simulations. We find that STI causes strain relaxation in the first 25nm of the channel, therefore affecting narrow devices much more than wide ones. Fig.2 shows the 375nm wide NMOS device with FUSI gates exhibits significantly higher (24%) mobility enhancement- compared to the unstrained case- due to the better stress conservation compared to the narrower 150nm device (13%). Investigation of the impact of the metal gate on the overall stress distribution shows that gate silicidation reduces useful longitudinal stress level by about 200 MPa. We investigate the effect of STI profile and also look into new trench filling material. Fig. 3 shows that the width effect can be drastically reduced if the trench is filled with a tensile film. Such an STI fill would also increase the longitudinal component of stress. The resulting strain would be equivalent to the strained silicon with 35% germanium content.

References: [1] Q. Xiang et al, VLSI 2003, p.101; [2] T. Sanuki et al, IEDM 2003, p.65

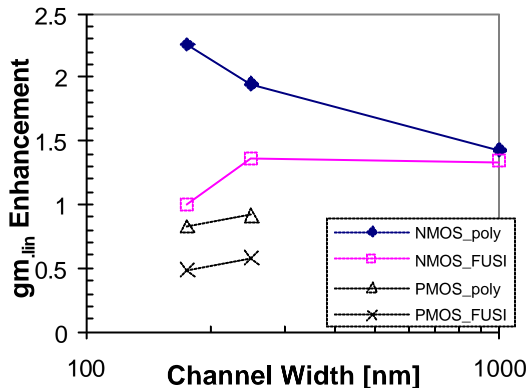

Fig.1: Enhancement of linear transconductance for 35nm strained devices with poly and FUSI gates for different gate widths.

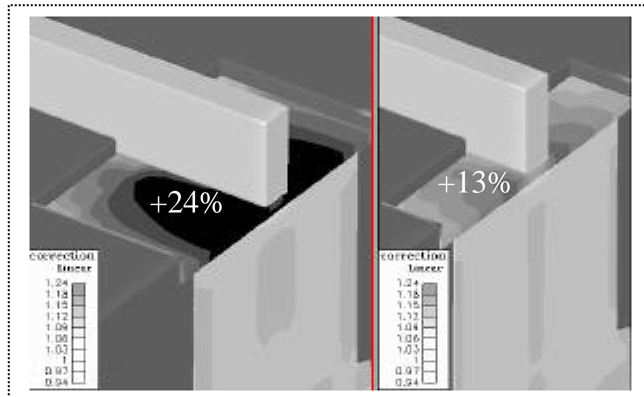

Fig.2: Local mobility correction using stress tensor for 150 and 375nm wide NMOS devices with FUSI gates.

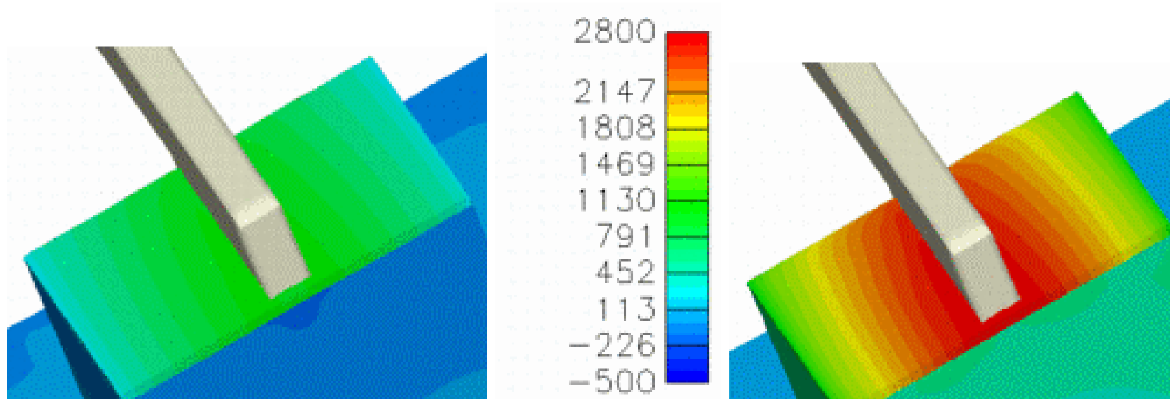

Fig.3: Contours of longitudinal stress for a strained NMOS (L=35nm,W=375nm) with no intrinsic stress in the STI fill (left) and tensile intrinsic stress (1GPa) in the STI fill (right).