Schottky Barrier Height Engineering with a Strained-Si channel for Sub-50-nm Gate Schottky Source/Drain MOSFETs.

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INTRODUCTION

The Schottky source/drain MOSFET (SSD-MOSFET) (1,2) is an attractive design for ballistic MOSFETs because it has the potential to allow high-energy carrier injection from a metal source to an intrinsic channel. This structure offers a new insight regarding nanoscale MOSFETs. However, achieving high-drive current is difficult because of the relatively high potential barrier (Schottky barrier) at the source. To overcome this problem, we have proposed Schottky-barrier-height (SBH) engineering through semiconductor bandgap modulation with the introduction of SiGe alloy and germanosilicide(3). However a simpler material system is preferable for mass-production SBH engineering.

In this paper, we demonstrate a new SBH engineering technique where strain is induced to lower the conduction and valence bands lowering of Si channel. We found the SBH at the source/channel junction could be modulated by tensile-stress applied to the Si channel. The current drivability of a strained-Si channel SSD-pMOSFET was thus improved partly from barrier reduction and partly from mobility enhancement.

DEVICE FABRICATION

Figure 1 is a TEM micrograph of a fabricated 50-nm-gate device. Epitaxial layers were a 2-µm-thick SiGe graded buffer, a 1-µm-thick relaxed SiGe buffer, and a 20-nm-thick strained Si channel. We intentionally left these layers undoped (< $1x10^{16}cm^{-3}$) and varied the Ge content (x=10, 20, or 34%) in the SiGe buffer layer for comparison. The source and drain junction-depths were about 12 nm. Platinumsilicide (PtSi) formed only within the strained-Si layer. The SiGe buffer layer was not silicided (It was confirmed by the SIMS depth profile).

DEVICE CHARACTERISTICS

Figure 2 compares the drain current curves of a 200-nm gate-length device with a Ge content of either 20 or 34%. A 61% improvement was observed for x=34% compared to x=20%. In addition, the G_m curves for devices at a low drain voltage (V_d= -0.05V) showed a significant increase in G_m (Fig. 3). These drive current and transconductance improvements were caused partly by the reduced barrier height for the strained-Si channel and partly by the higher mobility of holes in the strained-Si channel.

Figure 4 compares the gate length (L_g) dependence of I_{on} @V_d=V_g= -1.5V with various Ge contents. When L_g was 50nm, I_{on} for x=34% increased by more than sixfold compared with that for x=10%.

CONCLUSIONS

For the first time, we have demonstrated strained-Si channel SSD-MOSFETs. We also showed that strain can be used to reduce the SBH as an effective means of improving current drivability. By combining strained-Si channel SSD-MOSFETs with SSOI substrates (4), we can reduce the off-state leakage current and apply metal gate technology to adjust the threshold voltage. The strained-Si channel SSD-MOSFET is therefore a promising design for future nanoscale-MOSFETs.

REFERENCES

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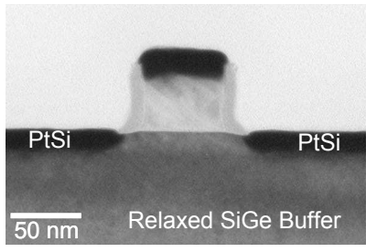

Fig.1. TEM micrograph of a fabricated 50-nm device.

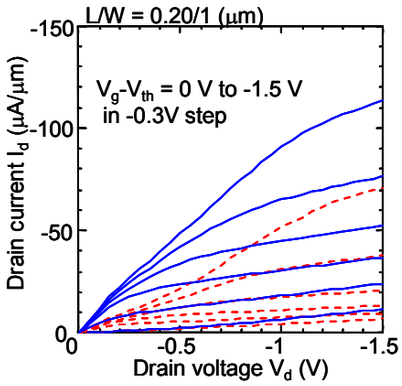

Fig.2. Drain current curves for 200nm gate-length devices with different Ge content. The solid and broken curves are for x=34% and x=20%, respectively.

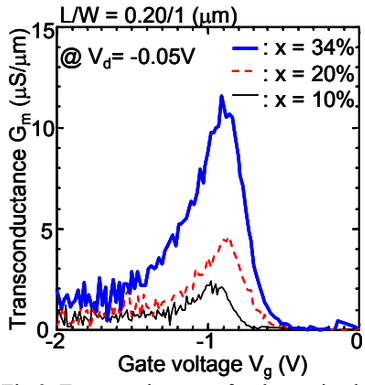

Fig.3. Transconductance for the strained-Si channel SSD-MOSFETs as a parameter of the Ge content.

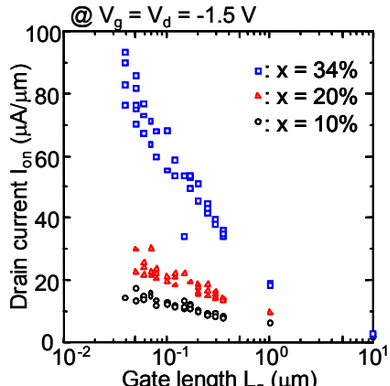

Fig.4. Gate length dependence of Ion for the different Ge content.