

Investigation of Facet Formation in RTCVD Si/SiGe
Selective Epitaxy

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Selective epitaxial growth is of a great interest for the integration of new CMOS devices (SON, SOI-FD, Double Gate...). In most of these applications, the morphology, especially the facets, has to be controlled. In this paper, we investigate the influence of growth parameters (temperature, GeH₄ and HCl partial pressures) and the nature of surrounding dielectric on the development of facets in the selective epitaxial growth of Si and SiGe.

The deposition was carried out by thermal decomposition of dichlorosilane in a 200mm wafers industrial cold-wall RTCVD reactor. For this study, we chose a very simple geometry that consists in Si active zone etched in thick dielectrics (SiO₂ or Si₃N₄). The dielectric walls are nearly vertical and the wafers have silicon and dielectric areas in the ratio 30%/70%. Each sample was chemically cleaned prior to loading and subsequently hydrogen baked. In order to observe the facet formation and propagation, we introduce SiGe markers grown at the same temperature than the silicon [1]. The measured angles of the facet are well correlated with the calculated value.

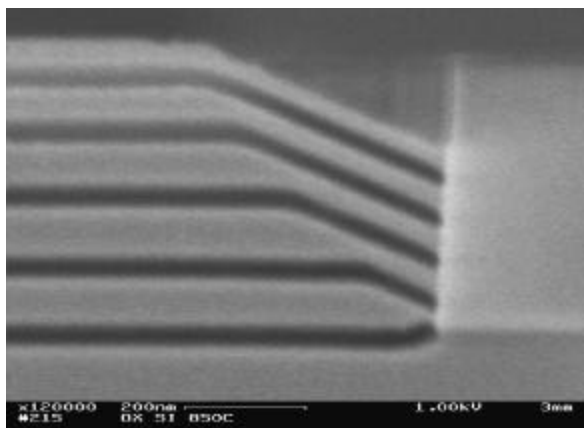


Fig. 1 SEM cross-section of selective epitaxial growth of Si at 850°C. with SiO₂ walls

In case of growth at 850°C, it is observed in figure 1 that clear facets are formed from the beginning of the Si growth [2]. These planes, characterized by an angle of 25.9° with {100} plan, are identified to {311} facets (25.2° theoretically). At this temperature, we also have measured a growth rate ratio of 0.53 between the {311} and {100} planes.

By reducing the temperature at 800°C and 750°C, we observe a reduction in the propagation of the facet. We also noticed that the growth rate ratio between {311} and {100} planes slightly increases with the temperature reduction: from 0.53 at 850°C to 0.67 at 800°C.

At 750°C, as illustrated in figure 2, no facet was observed. We have also noticed that the facets created by SiGe markers are eliminated by the silicon growth. This demonstrates clearly that facets can be limited or even eliminated by a temperature reduction, this however leads to a drastic growth rate decrease.

In part for this reason, a significant growth rate at a limited thermal budget, the SiGe alloy are often considered.

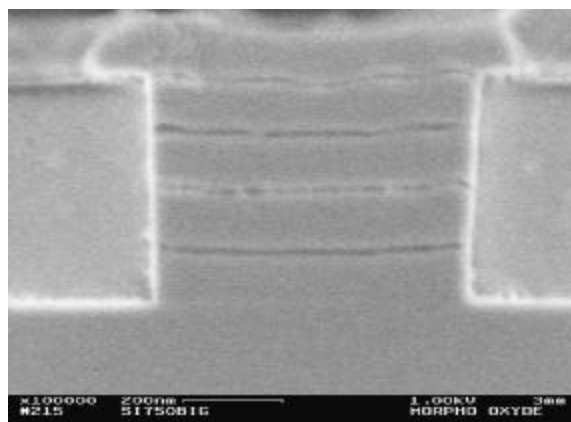


Fig. 2 SEM cross-section of selective epitaxial growth of Si at 750°C. with SiO₂ walls

In the case of SiGe growth (with Si markers) at 750°C, {311} and {111} facets (Fig. 3) are observed. So, at a given temperature and compared to silicon, the growth of Si_{0.85}Ge_{0.15} induces an increase of facet propagation compared to silicon. Again, by reducing significantly the temperature, the facets can be limited or eliminated: down to 600°C, we observed that {311} facets disappeared at 650°C and {111} facets disappeared at lower temperature. At 600°C, we do not observe facet formation with oxide

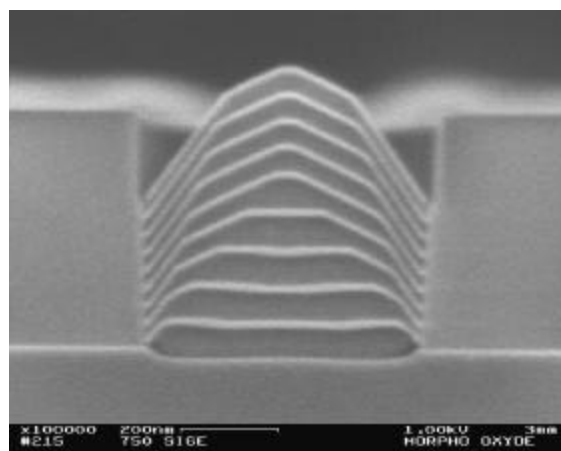


Fig. 3 SEM cross-section of selective epitaxial growth of SiGe at 750°C. with SiO₂ walls

In the same time of the investigation of the temperature, we have quantified dielectric and HCl partial pressure effect on the facets. In the range 850°C-650°C, we have observed that the facet planes are fixed by the temperature and the material (silicon or SiGe alloy). We have noticed that varying HCl flow or dielectric allow us to delay the formation of the facet.

In conclusion, we have observed that the temperature is a key parameter to reduce or eliminate the facet formation. If we want to use SiGe instead of Si chemistry, we also have to reduce drastically the temperature down to 600°C. By decreasing the temperature (750°C for silicon and 600°C for SiGe alloy), we obtain selective epi layers without facets for thickness exceeding 3000Å. In the same way, We have observed that the use of Si₃N₄ instead of SiO₂ delays the formation of facets and also reduces their lateral propagation

- [1] Vescan et al. J. Vac. Sci. Technol. B 16(3) (1998)
[2] A.Aoyama et al. J. Cryst. Growth 136 (1994) 349.