3D integration of ultimate devices thanks to SiGe.

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Abstract

The road to achieve the ultimate CMOS devices is now under wide investigation with the development of new architectures such as SOI (Silicon On Insulator), SON (Silicon On Nothing) or DG (Double Gate). These devices have thin conduction films. They give the best guarantee for the critical SCE and DIBL effects control for the last technologic nodes (defined by the ITRS roadmap).
In order to answer all the circuit requests and co-integrate different transistor families (HP, LP…etc.) we need to consider a lot of challenges:

- Development and optimization of the different device architectures: BULK, SOI, SON and DG (Planar, FinFet and/or Vertical configuration).
- Co-integration of these architectures on a same wafer.
- Co-integration, on the same chip, of different device configurations (for example Si channel for Nmos and SiGe channel for Pmos).
- Integration of new or existing materials as active layers or sacrificial layers for channel, gate and/or source /drain realization. It is also possible to use the different properties of the crystalline orientation or modify the stress induced on the devices.
- Density consideration (how can we reduce the dimension of the pitch?) for the memories and logic cells.

Because of all these considerations, we propose to use a 3 Dimension approach. Usually transistors are built step by step, by simple layer superposition. Now the new 3D challenge requests to work with buried sacrificial layers to use the free space left in the substrate and the different isolation films. Actually, only few materials can be used as sacrificial layers: knowledge of selective etching and selective deposition of SiGe makes it one of the best candidates for addressing the new SIS (Something Instead Something) concept.
Concrete realization of this concept has already been demonstrated by the following achievements:

- The GAA fabrication [1]: a multi-layer stack has been realized thanks to the replacement of the SiGe sacrificial layer by poly-silicon. In these devices, by simple epitaxy, we can achieve a Silicon channel (Fig.1) or a Silicon Germanium channel, both mono-crystalline. Simple lithography allows combination of both material channels on the same chip. Thanks to the Silicon On Nothing (SON) process, performant double gate devices have been realized in a planar configuration (Fig.2). We can also notice that if we are able to decouple the two gates, two independent MOSFET can be realized, optimizing 3D density integration.
- The PRETCH realization [2] where the poly-silicon-germanium or the poly-silicon is used as a sacrificial film for a mid-gap gate fabrication. 3D density optimization was achieved with the realization of transistors with high-K oxide combined with a metal gate by deposition through the contact holes (Fig.3). This new integration allows low thermal budget for the high-K film (deposited after source and drain anneal), no particular contamination issues (back-end steps) and easy dual gate and/or dual gate oxide realization for CMOS application.

All the potential of the Something Instead of Something (SIS) concept is also demonstrated by addressing the density and coupling challenges for the memories and logic functions.

References:

[1] S.Harrison *et al*, IEDM Tech.Dig., 2003, p.449
[2] S.Harrison *et al*, INFOS Tech.Dig., 2003.

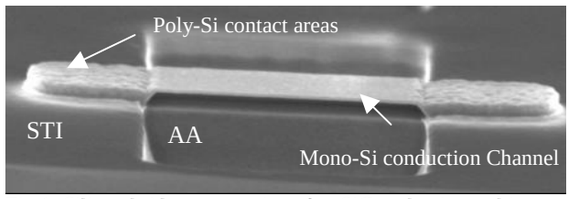

Fig 1: Silicon bridge over active after SiGe selective etching

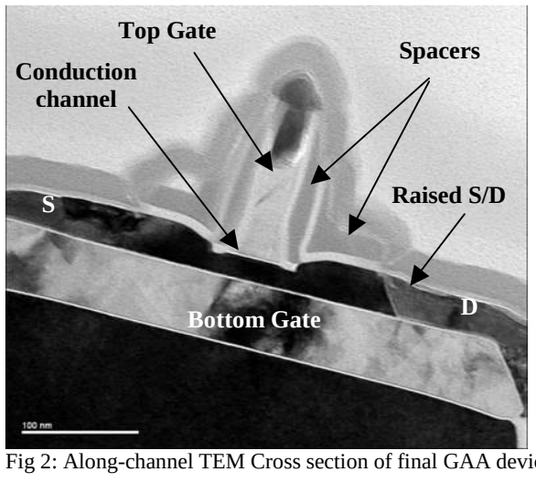

Fig 2: Along-channel TEM Cross section of final GAA device

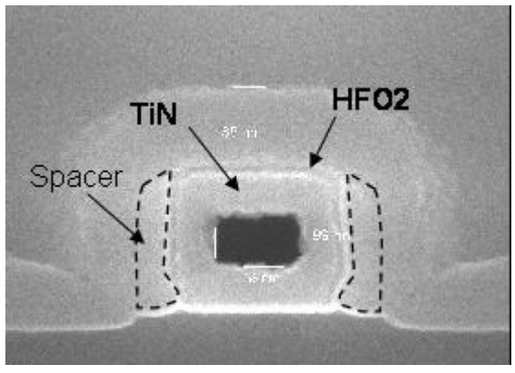

Fig 3: View of transistor gate after tunnel filling by 450A TiN and 60A HFO2.