Abs. 1354, 206th Meeting, © 2004 The Electrochemical Society, Inc.

SiGe-based Combined MBE and CVD Processing for Vertical Silicon-on-Nothing (SON) Device Technology

J. Schulze, I. Eisele, P.E. Thompson[1], G. Jernigan[1], T. Suligoj[2]
University of the German Federal Armed Forces Munich, Institute of Physics (EIT 9.2), Neubiberg Germany
[1]Naval Research Laboratory, Washington, DC, USA
[2]University of Zagreb, Department of Electronics, Zagreb, Croatia

INTRODUCTION

To study the behavior of partially- or fully-depleted metal-oxide-semiconductor field-effect transistors (PD/FD-MOSFETs) with channel dimensions in the sub- or ultra-sub-*30nm* regime only standard technology combined with cost-intensive "Silicon-on-Insulator" and e-beam lithography is available at the moment. An interesting alternative approach is given by "Silicon-on-Nothing" (SON) concepts recently discussed for lateral partially- or fully-depleted MOSFETs [1, 2]. In this contribution we want to introduce a novel SiGe-based vertical SON technology for the fabrication of PD/FD-MOSFETs in this regime.

SONFET CONCEPT

We have developed a combined molecular beam epitaxy (MBE) and chemical vapour deposition (CVD) process based on selective SiGe etching for the fabrication of vertical, fully depleted SON-MOSFETs (VFD-SONFETs) with channel length L and depletion width W_D in the sub-30nm regime defined by atomically controlled deposition instead of lithography. The transistor width W is defined by optical lithography.

As depicted in fig.1 the basic structure for a n(p)-channel VFD-SONFET is a SiGe sacrificial layer and a $n^+(p^+)$-doped Si top layer working as source deposited by means of MBE on top of a $n^+(p^+)$-doped Si substrate (drain). The thickness of the SiGe layer determines the channel length L of the final VFD-SONFET.

After mesa etching (which is an uncritical lithography step) an ultra-thin intrinsic Si layer is conformal deposited by means of CVD (its thickness determines the depletion width W_D). After conformal deposition of an Al_2O_3 gate dielectric by means of Metal-Organic CVD (MOCVD) a highly $n^+(p^+)$-doped polycrystalline Si layer is deposited using Low Pressure CVD (LPCVD). After gate electrode formation the MOS gate is encapsulated with a SiO_2/Si_3N_4 passivation layer, the transistor body is opened by reactive ion etching (RIE), and the SiGe layer is etched away with a selective SiGe etch. Finally an overall SiO_2/Si_3N_4 capsule and metal contacts are formed (fig.2).

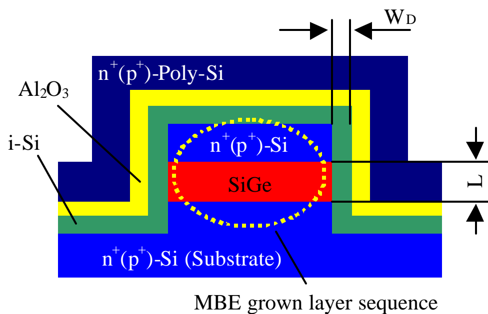

Fig.1: Fabrication of the proposed n(p)-channel VFD-SONFET before selective $Si_{1-x}Ge_x$ removal

To avoid the collapse of the transistor body after SiGe removal the top electrode must be realized as cantilever, bridge, or trench structure.

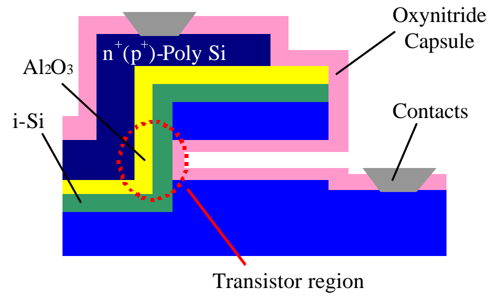

Fig.2: Proposed n(p)-channel VFD-SONFET

RESULTS

A critical step in the processing sequence is the selective removal of the SiGe under the gate. We have used a PA:HF:H_2O = 1:1:1 solution (PA: Peracetic Acid, HF: Hydrofluoric Acid) and a high selective removal of the SiGe was obtained, as can be observed by the bridge test structure in Fig.3.

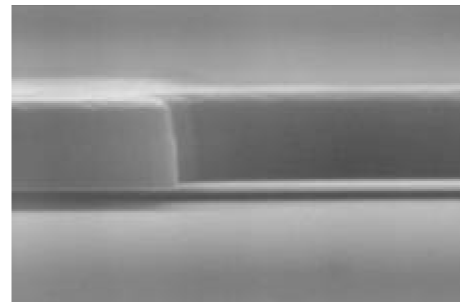

Fig.3: Complete undercutting of a 100nm $Si_{0.7}Ge_{0.3}$ layer

The SiGe layer had a thickness of *30nm*, *50nm*, or *100nm* and a *30%* Ge composition. Si deposition for channel formation was *30nm*. Different test device configurations, such as a trench structure, bridge structures (fig.4), and cantilever structures were fabricated.

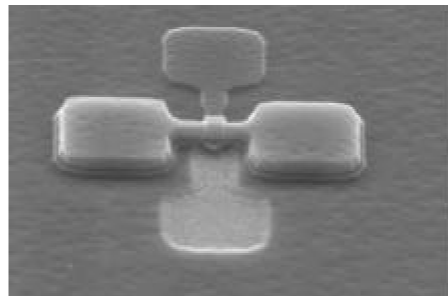

Fig.3: SEM of a VFDSONFET without gate structure and capsule after selective SiGe etching (bridge structure)

The top n^+-region (source) is mechanically stable after the SiGe layer etching step up to the lengths >*5µm*, which makes it possible to process wide and/or multiple gate fingers. The complete fabrication sequence involving an ion implanted drain, MBE-grown SiGe sacrificial layer and n^+-doped contact layer, mesa etching, CVD of Si for channel formation, selective SiGe etching, gate and contact formation will be discussed.

References

[1] Monfray, Skotnicki, Tavel, Morand, Descombes, Talbot, Dutartre, Jenny, Mazoyer, Palla, Leverd, LeFriec, Pantel, Haond, Charbuillet, Vizioz, Louis, Buffet, Tech. Dig. IEDM-2002, 263 (2002)
[2] Sato, Nii, Hutano, Takenaka, Hayashi, Ishigo, Hirano, Ida, Aoki, Ohguro, Ino, Mizushima, Tsunashima, Tech. Dig. IEDM-2001, 809 (2001)