

## “Strained silicon on silicon by wafer bonding and layer transfer from relaxed SiGe buffer”

David M. Isaacson, Gianni Taraschi, Arthur J. Pitera, Nava Ariel, and Eugene A. Fitzgerald  
Department of Materials Science and Engineering,  
Massachusetts Institute of Technology  
Cambridge, MA 02139

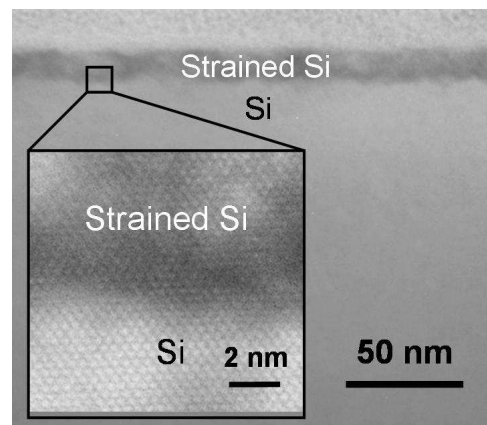
Thomas A. Langdo  
AmberWave Systems Corp.  
Salem, New Hampshire 03079

Strained silicon heterostructures have been shown to provide significantly enhanced carrier mobilities over their bulk Si counterparts [1,2]. Once a strained layer of Si has been created, there are many new materials platforms that can take advantage of the superior electronic properties of strained Si, including strained Si on SiGe [3], silicon-germanium on insulator (SGOI) [4-7], and most recently strained-Si on insulator (SSOI) [8]. While all of these materials can provide significant performance enhancement in CMOS devices through enhanced carrier mobilities relative to bulk Si, implementation of all of the materials listed requires some level of modification to existing device processing methods due to either the presence of either Ge or an insulating layer.

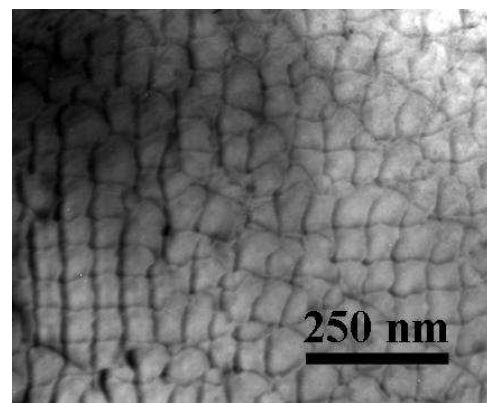
Additionally, applications using high-power devices require extraordinary heat removal, and heat removal through the substrate is reduced due to the lower thermal conductivity of SiO<sub>2</sub> and SiGe. Local temperature increases near the device channel can lead to loss of mobility and a reduced drain current [9]. Temperatures in SOI devices, for example, have reportedly increased as much as 100 K under static conditions [10].

An alternative to the relaxed SiGe, SGOI, and SSOI platforms would be to incorporate a strained silicon layer directly on a bulk Si wafer without an intermediate SiGe or oxide layer. We report the creation of strained silicon on silicon (SSOS), which avoids the interdiffusion, contact metallurgy, and self-heating issues of the platforms listed above, making SSOS a direct substitution for silicon substrate.

We fabricated strained silicon on silicon (SSOS) using a wafer bonding and layer transfer process. A strained silicon layer on relaxed SiGe graded buffer was bonded to another silicon wafer, the final structure of which is shown in Figure 1. As can be seen from the inset in the Figure, the interface is oxide-free and of very high quality. Retention of the strain in the strained Si layer is implied by the presence of a misfit dislocation array which accommodates the lattice-mismatch between the strained Si layer and the Si substrate, as shown in Figure 2. A more detailed analysis of the dislocation network as well as potential implications of this network on device performance will be presented.



**Figure 1** - Cross-sectional TEM image of the SSOS structure. Shown at inset is a high-resolution image of the interface.



**Figure 2** - Plan-view TEM image of the strained silicon / silicon interface.

### References:

1. J. Welser, J. Hoyt, S.-I. Takagi, and J. F. Gibbons, Tech. Dig. - Int. Electron Devices Meet. **1994**, 373 (1994).
2. M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, J. Vac. Sci. Technol. B **19**, 2268 (2001).
3. Y.-J. Mii, Y.-H. Xie, E. A. Fitzgerald, D. Monroe, F.A. Thiel, B. E. Weir, and L. C. Feldman, *Appl. Phys. Lett.* **59**, 1611 (1991).
4. S. Fukatsu, Y. Ishikawa, T. Saito, and N. Shibata, *Appl. Phys. Lett.* **72**, 3485 (1998).
5. L. J. Huang, J. O. Chu, D. F. Canaperi, C. P. D’Emic, R. M. Anderson, S. J. Koester, and H.-S.-P. Wong, *Appl. Phys. Lett.* **78**, 1267 (2001).
6. Z. Cheng, G. Taraschi, M. T. Currie, C. W. Leitz, M. L. Lee, A. Pitera, T.A. Langdo, J. L. Hoyt, D. A. Antoniadis, and E. A. Fitzgerald, *J. Electron. Mater.* **30**, L37 (2001).
7. T. Tezuka, N. Sugiyama, and S. Takagi, *Appl. Phys. Lett.* **79**, 1798 (2001).
8. T. A. Langdo, M. T. Currie, A. Lochtefeld, R. Hammond, V. K. Yang, J. A. Carlin, C. J. Vineis, G. Braithwaite, H. Badawi, M. T. Bulsara, and E. A. Fitzgerald, IEEE International SOI Conference Proceedings, 2002, p. 211.
9. A.L. Caviglia, A.A. Iliadis, *IEEE Electron Device Lett.* **14**, 133 (1993).
10. L.T. Su, J.E. Chung, D.A. Antoniadis, K.E. Goodson, M.I. Flik, *IEEE Transactions on Electron Devices*, **41**, 69 (1994).