Outlook and opportunities for hetero-epitaxy in Si CMOS technology and beyond

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Introduction. The introduction by IBM of a production SiGe HBT technology in 1998 marked a major advance in microelectronics, not only because it lead to the emergence of silicon in the communications marketplace, but, for the first time, it demonstrated the commercial viability of Si-based hetero-epitaxial devices. Despite similar promise for success, mainstream CMOS technology has been slow to adopt SiGe hetero-epitaxial devices. However, as conventional device scaling runs out of steam, this attitude is changing, and hetero-epitaxy is being considered for a variety of uses in standard CMOS devices. Here, I will review the most promising applications of Si/SiGe hetero-epitaxy for mainstream CMOS technology. I will also briefly describe other emerging Si-based heterostructure devices that could be enabled by the widespread availability of Si-based hetero-epitaxy.

SiGe raised source-drain. The simplest hetero-epitaxial solution that is likely to emerge in commercial CMOS technology is SiGe raised-source drains (RSD) (1). Though not technically a heterostructure solution (the band offset is not explicitly implemented for device performance), SiGe RSD has the benefit of reducing contact resistance compared to Si homo-epitaxial RSD, due to the reduced Schottky contact barrier height. The increased Ge concentration also allows reduced growth temperature compared to Si RSD, an important consideration to minimize dopant diffusion. One challenge for SiGe RSD implementation is the effect of Ge on Co silicide formation. Even small amounts of Ge can dramatically increase the transition temperature for the low-resistance disilicide ($CoSi_2$) phase. Possible solutions to this problem are the utilization of a sacrificial Si cap layer, or the use of NiSi as the contact material.

Strained Si MOSFETs. The main application of Si/SiGe hetero-epitaxy in Si CMOS devices is the growth of biaxially tensile-strained Si on relaxed $Si_{1-x}Ge_x$ for strained Si CMOS (2). The strained Si surface channel provides enhanced carrier mobility for electrons, and when $x > 30\%$, for holes as well, and the higher mobility leads to improved current drive compared to unstrained Si. The prototypical strained Si MOSFET requires the formation of a relaxed SiGe underlayer. Though the various methods of forming relaxed SiGe will not be discussed here, a common aspect of these layers is that they have a finite number of defects (e.g. threading dislocations, stacking faults). It is these defects and their potential effect on device yield and reliability that has been the main obstacle to the implementation of strained Si on SiGe CMOS in manufacturing. Epitaxy for strained Si MOSFETs is needed to grow strained Si on the relaxed SiGe substrate. The main requirements for strained Si epitaxy are control of the Si thickness and low regrowth interface contamination. Thickness control is particularly important for highly-strained systems, where the Si must be sufficiently thick to accommodate process-induced Si loss and Ge outdiffusion from the relaxed SiGe layer, while remaining thin enough to prevent defect formation during processing. At higher Ge concentrations, cleaning of the regrowth interface is more difficult and interface contamination can lead to nucleation of new defects in the regrown film. Similar to SiGe RSD, strained Si on relaxed SiGe MOSFETs are not true heterostructure devices, in that the sole purpose of the SiGe is to strain the Si; the heterojunction has no intended function. As a result, simpler methods of producing strain, such as local stress from dielectric layers and embedded SiGe, remain the up-front approaches for manufacturing strained Si CMOS. The latter technique (3) is particularly attractive, as it utilizes selective SiGe epitaxy in the source and drain regions, but avoids the formation of blanket relaxed SiGe.

Buried-channel MOSFETs and MODFETs. Unlike surface-channel strained Si MOSFETs, buried-channel devices utilize strain-induced band offsets for carrier confinement and therefore require the use of hetero-epitaxy. Buried-channel devices are of interest to increase the carrier mobility compared to surface-channel devices by eliminating surface-roughness scattering. Buried SiGe layers grown on Si have been proposed for enhancing pFET mobility, but the anticipated performance advantages are marginal. Greater hole mobility enhancement can be obtained by using buried $Si_{1-y}Ge_y$ layers grown on relaxed $Si_{1-x}Ge_x$, where $y > x$. Such structures can produce hole mobility enhancements as high as 10-12 (4), which may be sufficient to overcome the transconductance penalty due to the reduced gate capacitance. In these types of devices, monolayer thickness control is paramount, because the population ratio of the surface and buried channels is highly sensitive to the depth of the quantum well below the surface.

The introduction of modulation-doping provides an alternative way of populating buried-channel devices. Both p-and n-MODFETs can be made by producing buried-channel heterostructures with remote doping introduced *in situ* during epitaxial growth (5-6). The introduction of boron doping for p-MODFETs is relatively straightforward, and is already a well-established technique used for SiGe HBTs. Doping for n-MODFETs is more challenging, due to the difficulty in obtaining abrupt doping profiles and dopant memory effects, particularly for phosphorous doping. Both inter-wafer and intra-wafer doping uniformity is a concern for MODFETs. These epitaxial challenges, along with the thermal budget limitations of MODFETs and high-Ge content layers remain as barriers to manufacturability.

Optoelectronics and novel devices. Integrated optoelectronic devices are a potentially important area where the benefits of SiGe hetero-epitaxy have yet to be fully realized. For instance, Ge photodiodes can be fabricated using direct growth of Ge on Si for operation at near-infrared wavelengths (7). The defect density can be reduced by high-temperature annealing or selective-area growth, but extreme efforts to reduce the defects are not necessary since photodetectors appear to be more tolerant to defects than FETs. A great opportunity also exists for novel hetero-device engineering, if strained Si on relaxed SiGe becomes the *de facto* CMOS platform. Such devices include interband and intraband resonant-tunneling diodes which could have applications in novel logic and memory schemes. Optical emitters such as quantum cascade lasers (8), for mid-infrared and terahertz imaging applications could also be enabled by the widespread availability of Si/SiGe hetero-epitaxy and strained Si CMOS.

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