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Low-temperature CVD of epitaxial Si and SiGe layers: Room for improvement

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Low-temperature CVD of epitaxial and polycrystalline Si and SiGe layers has become an accepted technique to grow all sorts of complicated doping profiles. The capability of a standard production reactor to grow high quality Si and SiGe epi layers at low temperatures came as a surprise more than a decade ago and contrasted with UHVCVD, the preferred technique during those days.

The reactor under consideration was the first one of a new generation, characterized by single-wafer processing, a lamp-heated rotating susceptor and load-locked wafer entry. This last feature was especially important as it kept oxygen and moisture away from the process tube, allowing the growth of epi layers of excellent crystalline quality at conditions that are very relaxed compared to UHVCVD.

In the meantime the growth of Si/SiGe epi-layer stacks has become a routine in common single-wafer reactors and it seems that we got used to and take for granted some characteristics of this growing method that are not so good. Listed below in ascending order of importance are some areas of concern where improvements would be welcome.

Pre-epi hydrogen bake step

In contrast to UHVCVD a bake step is used during low-temperature epi in single-wafer reactors to remove the native oxide and to prepare the surface for epi growth, similar to conventional epi. Originally there was quite some concern that the temperature of the bake step could damage the structures already present on the wafer, as the temperature of the bake step is considerably higher than the growing temperature (typically 700°C). Over the years it turned out that the bake temperature could be lowered. 800°C is a common bake temperature now and there are good indications that even 700°C may work.

It still would be nice to have an alternative and more robust way of cleaning the wafer at a temperature at or below the deposition temperature, but the drive to develop an HF vapor clean or a plasma clean has decreased considerably.

Throughput

In every single-wafer reactor the growth rate is a concern. However, the throughput of multi-layer structures consisting of many thin layers, like a typical HBT Si/SiGe/Si stack, is more limited by the number of layers than by the growth rate. The growth rate of SiGe, boosted by the presence of GeH_4, is usually high enough. The growth rate of Si can be adjusted by choosing the proper precursor. In ascending order: SiH_2Cl_2 – SiH_4 – Si_2H_6 – Si_3H_8. Some care should be exercised as the precursors with the highest growth rates also have the highest tendency to coat the quartz process tube.

Only when thick layers have to be deposited (relaxed buffer layers) the growth rate becomes a real concern. Unless alternative deposition methods are developed, this is not something that can be done economically in a single-wafer reactor.

Besides process improvements there is a hardware improvement that would be very beneficial to the throughput. Getting rid of the low thermal mass susceptor, switching to real susceptorless epi, would shorten each run by several minutes. The bottleneck is how to measure the wafer temperature.

Metrology

Conventional methods to measure epi layers, like FTIR and four-point-probe, cannot be used to determine the characteristics of thin multi-layers with complicated doping profiles. Instead SIMS is used to determine the layer thickness and the doping levels. Although we are depositing the heart of a transistor which characteristics depend critically on layer thickness, Ge content and doping level, ironically our evaluation equipment is inferior compared to what we are using in conventional epi growth. A repeatability of better than 1% for FTIR and 4-point probe is replaced by SIMS with a repeatability of 5-10% at best. Optical spectroscopy to monitor the process on a continuous basis comes in handy but is insufficient, as it only measures the layer thickness and the Ge content.

What saves us here is the long term stability of the reactor. The reactor, when left untouched, is more stable than the measurements. Even so, the robustness of any low-temperature epi process would benefit from metrology improvements.

n-Type doping

Being used to the box-shaped profiles of Ge, B and C in low-temperature epi and the easy tuning of any odd profile, the poor control over n-type dopants (As and P) is a disappointment. The surface segregation effects of these dopants cause very long tails when the AsH_3 or PH_3 gas flows are switched off. This phenomenon is shared by low-temperature CVD, UHVCVD and even MBE. The fact that the problem does not depend on the deposition method already indicates that it is a characteristic inherent to the used chemical that will be hard to beat.

The only relief comes from using PH_3, rather than AsH_3, at atmospheric pressure. Moderately steep P profiles are possible under these conditions, albeit that growth at atmospheric pressure is usually not the preferred mode.

Emissivity effects

In epi reactors which measure and control the susceptor temperature rather than the wafer temperature, with a thermocouple or otherwise, the deposition parameters suffer from temperature variations. Anybody working with these types of reactors learns very soon that test runs made at reduced pressure on virgin wafers show growth rates and doping concentrations that differ considerably from similar runs made on patterned wafers. Behind these discrepancies are temperature variations caused by varying wafer emissivities. The temperature shifts can be dramatic, 30-50°C difference between a patterned and an unpatterned wafer is possible. Even worse is that during blanket deposition on a patterned wafer the emissivity, and consequently the wafer temperature, changes during the deposition.

The effects on the deposition parameters are manifold: the layer thickness does not respond linearly to the deposition time, the doping levels are not constant and a pattern change requires recalibration runs.

There is a straightforward solution to these problems: direct measurement and control of the wafer temperature. The practical implementation is not as easy as it may seem, though.