# High-Quality Strain Relieved SiGe Buffer Prepared by Means of Thermally-Driven Relaxation and CMP process

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## *1. Introduction*

Fully relaxed SiGe buffer layer is of increasing issue for the fabrication of future Si large-scale-integrated applications, since both electron and hole mobility are expected to be largely enhanced. It is important to control the process parameters for the growth and the design of buffer layer structures in order to minimize the density of threading dislocations(TDs) extending to the surface of a relaxed buffer layer. The conventional method utilizing graded SiGe growth as thick as several μm, has dis-advantages of long growth time, materials consumption, and the large step height of hetero devices.

In this paper, we proposed a new method to obtain high-quality strain-relaxed SiGe buffer layers on Si(100) by TDR(thermally driven relaxation) and CMP(chemical mechanical polishing) technique.

## *2. Fabrication Processes*

TDR growth is composed of two parts. At first, a compositionally graded layer is grown at low temperature up to a certain value of Ge mole fraction and the intermediate annealing were performed without source gas flow using high ramping rate of RPCVD. The MDs(misfit dislocations) are not restricted to only one interface but have space to spread over the thickness range of the graded layer with low TD density on the surface. So, it is considered that high temperature cyclic heat treatment steps during the growth of graded SiGe buffer layer help to annihilate TD arms. After the constant SiGe layer of 1um, we annealed the sample at 1100□ for 1hour to enhance the degree of relaxation and enlarge the thermal budjet. We also flattened the rough surface of the strain-relaxed SiGe buffer layers by CMP and successfully obtained the ultra-smooth surface, where the root mean square roughness was about 1nm with less than $10^5/cm^2$ of TD density. Fig. 1 shows a schematic drawing of SiGe buffer. The growth temperature of SiGe buffer layer was 600□ and the 4-cycles TDR step at 950□ was added in graded SiGe buffer layer 50nm at each 5% increase of Ge content.

## *3. Morphology and Relaxation Properties*

AFM images are shown in Fig. 2. Clearly defined surface cross-hatch patterns were observed which is consistent with effective strain relief through MDs by the modified Frank Reed(MFR) mechanism. AFM measurements yielded an RMS roughness of 38.2nm before CMP process and 1.2nm after re-growth of SiGe layer with CMP process. Fig. 3 exhibits the structure of the dislocation networks in the buffer as observed by cross-sectional TEM. The MDs are arranged in different planes that are connected by TDs. Above this network exist a perfectly grown layer almost free of TD. Secco-etched sample images to estimate the TD density resulted in about $8\times10^4/cm^2$, which is very low value for the reported SiGe graded buffer layer.

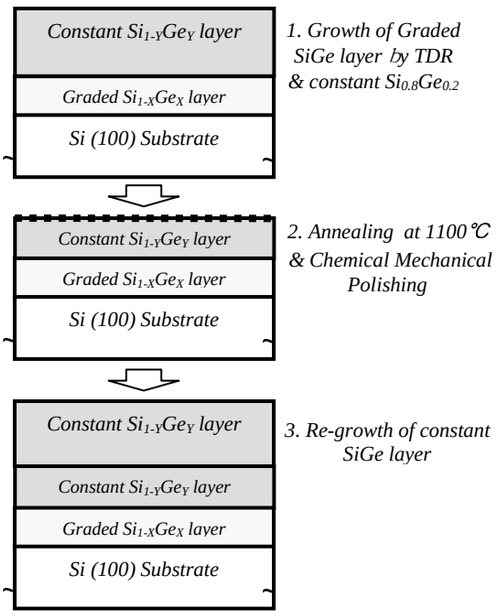
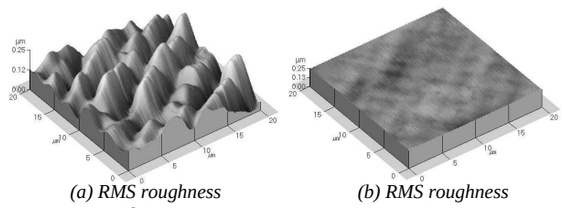



**Fig. 1.** Schematic cross-section of thin SiGe buffer

Summarizing the results, TDR steps during the graded SiGe layer proved correct in order to minimize the TD density less than $10^5/cm^2$ with nearly 100% degree of relaxation and CMP process successfully help to obtain the ultra-smooth surface. Therefore, it is concluded that the cyclic TDR, if performed precisely at high-temperature, and CMP process would be useful in achieving SiGe relaxed layers with thicknesses below 1μm with smooth surface.



*(a) RMS roughness = 38.2nm* *(b) RMS roughness = 1.2nm*

**Fig. 2.** AFM images of the surfaces of the $Si_{0.8}Ge_{0.2}$ buffer layer (a) before CMP and (b) regrowth of SiGe layer after CMP

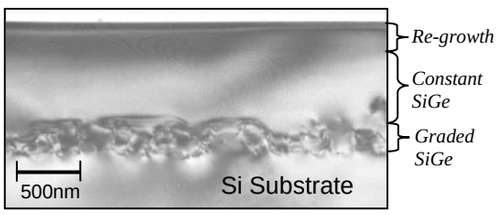



**Fig. 3.** Cross-sectional TEM image of $Si_{0.8}Ge_{0.2}$ buffer layer

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