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Growth and morphological stability of nickel germano-silicide on strained $Si_{1-x}Ge_x$ (x=0.1 to 0.25) under rapid thermal annealing

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SiGe alloys are very attractive for the future VLSI technologies such as raised source/drain for sub-micron CMOS. For SiGe device integration, a good metal/SiGe ohmic contact is required to maintain the device performance (1). Nickel germanosilicide, formed by interfacial reaction of Ni with $Si_{1-x}Ge_x$ layer, is one of the most promising candidate for low-resistant contacts on SiGe.

In this paper, we investigated the thermal reaction of Ni with 25nm of epitaxial $Si_{1-x}Ge_x$ (x=0.1; 0.15 ; 0.2 and 0.25) on Si(001) in the temperature range of 350-600°C for Ni thickness varying from 6 to 21nm. A particular attention has been paid to the influence of Ge content x and Ni initial thickness on Ni(SiGe) morphological stability. Results are compared with nickel silicide formed on Si(001).

Firstly, we studied the reaction between a 9nm Ni layer deposited on $Si_{1-x}Ge_x$. With such a Ni thickness, $Si_{1-x}Ge_x$ layers are not totally consumed by the silicidation. After thermal annealing, the nickel germanosilicide formed on epi-$Si_{1-x}Ge_x$ layers shows higher sheet resistance than that of NiSi on Si(001) substrate (figure 1a). For Ni(SiGe), lowest Rs values are obtained for layers annealed between 400 and 450°C, while a larger temperature range is allowed for NiSi. Since no $NiSi_2$ formation is detected until at least 700°C according to XRD analysis (figure 1b), the resistance degradation observed for annealing temperatures above 450°C is mainly due to Ni(SiGe) agglomeration. This is confirmed by SEM observations (figure 2). Preceding this agglomeration, micro-voids formation occurs as of 450°C, as previously shown by Yang et al. (2), but this phenomena does not affect the Rs stability. We also show that the formation of voids increases with Ge content (figure 3).

Finally, we investigated the influence of nickel thickness on Ni(SiGe) composition and surface morphology. When Ni thickness is lower than 15nm (i.e. $Si_{1-x}Ge_x$ layer is not entirely consumed by silicidation), the Ge profile through the Ni(SiGe) layer is not uniform : a higher Ge content is observed at the Ni(SiGe)/$Si_{1-x}Ge_x$ interface (figure 4). As Ni thickness increases, the Ge profile becomes more uniform, while the formation of voids becomes less important (SEM micrographs not shown here).

All these results will be discussed in details in the paper and compared to the literature.

REFERENCES

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(2) T.-H. Yang, G. Luo, E. Y. Chang, T.-Y. Yang, U.-C. Tseng and C.-Y. Chang, IEEE Electron Device Letters, 24(9), 544, (2003)

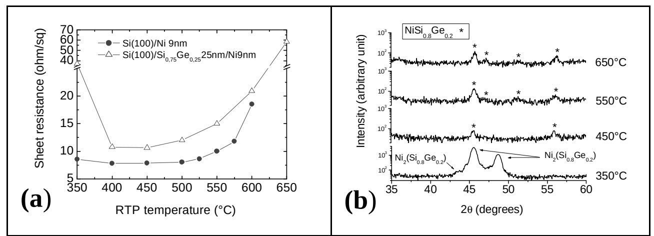

Figure 1 : sheet resistance (a) and XRD θ/2θ patterns (b) as a function of Rapid Thermal Annealing temperature of Ni 9nm/Si1-xGex (x=0 and 0.25) 25nm films. RTA is performed for 60s in an Ar ambient.

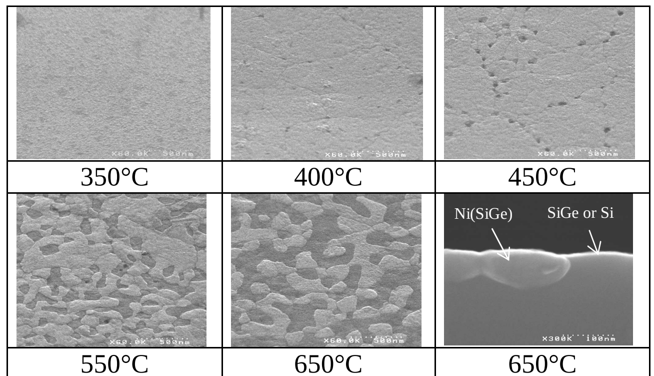

Figure 2 : top-view and cross sectional SEM micrographs of Ni9nm/$Si_{0.75}Ge_{0.25}$ 25nm samples annealed at different temperatures. Top-view pictures are tilted at 60°

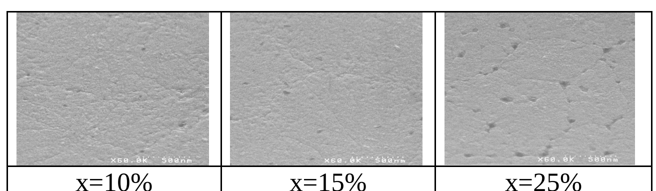

Figure 3 : top-view SEM micrographs (tilted at 60°) of Ni9nm/$Si_{1-x}Ge_x$ 25nm samples annealed at 450°C for 60s in Ar ambient for different x values

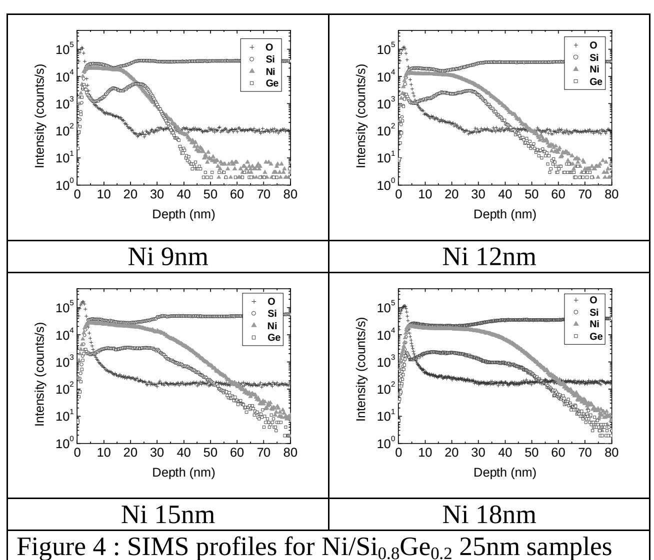

Figure 4 : SIMS profiles for Ni/$Si_{0.8}Ge_{0.2}$ 25nm samples annealed at 450°C for different Ni thickness