

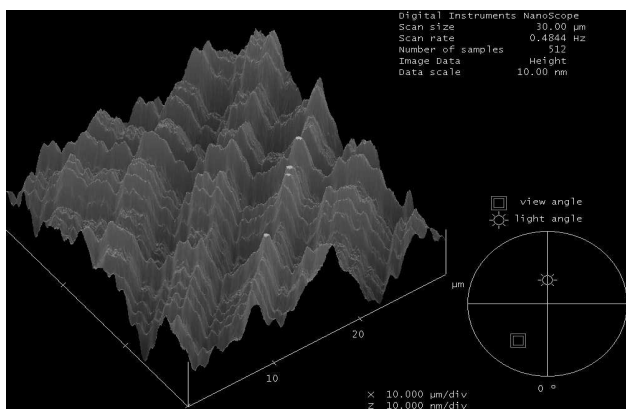
Minimizing Micro-Roughness of Strained Silicon Surfaces Without CMP

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Detailed characterisation of strained silicon surfaces indicates that the roughness features present are comprised of several distinct length scales. Surface micro-roughness is strongly dependent on the relaxed buffer layer quality and is driven by both long scale (low frequency) and short scale (high frequency) components (fig. 1). Surface characterization requires use of AFM scan sizes consistent with the length-scales of the features present. This enables the epitaxy process to be tuned to reduce both the long scale and short scale components.

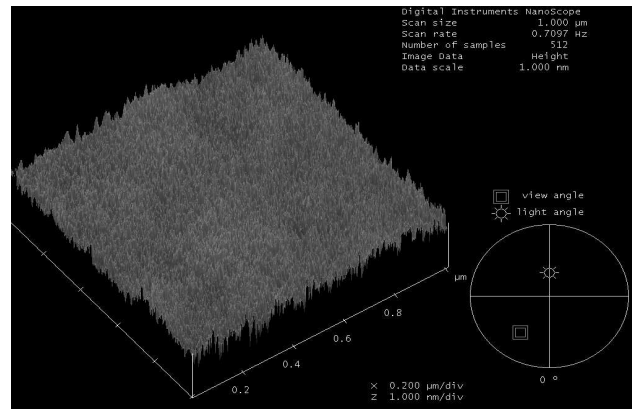
Figure 1. Non-optimized sSi - 30um AFM scan



At the advanced technology nodes where strained silicon materials are being evaluated it is important to reduce the short scale “nano-roughness”. This type of roughness is more relevant to device performance than roughness associated with longer scale features such as crosshatch. This is due to the fact that for deeply scaled MOSFETs the very high fields in the channel pull the carriers closer to the Si / gate dielectric interface where scattering due to surface roughness will degrade mobility.

AFM scans of strained silicon surfaces produced with an optimized growth process shows significant reduction in surface micro-roughness. RMS values below 1Å are achieved for 1um x 1um scan on polish-free material

Figure 2. -Optimized sSi - 1um AFM scan



Power spectral density data for 30um and 1um AFM scans (figs. 3 and 4) are shown for optimized and non-optimized processes. The frequency of features which contribute to the PSD (at all wavelengths within the resolution capability of the AFM) is reduced for the optimized process.

Figure 3. Power Spectral Density 30um Plot

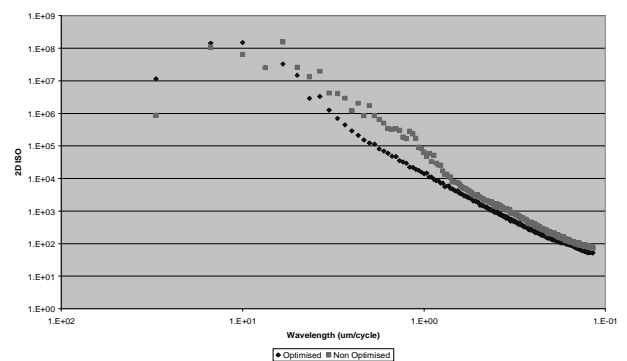
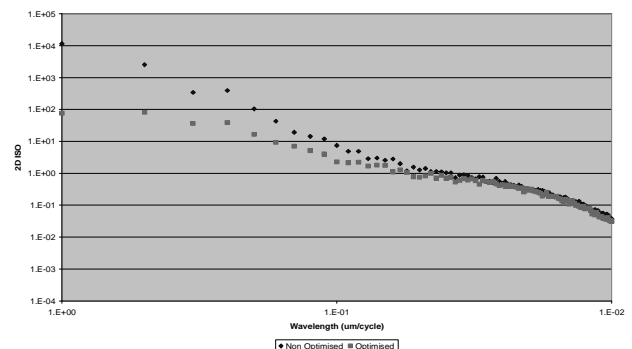


Figure 4. Power Spectral Density 1um Plot



Mobility and yield results for 70nm devices fabricated using unpolished strained silicon will be presented to demonstrate that CMP-free strained silicon is a cost-effective material suitable for leading edge technology nodes.

(Data from IQE's fab partner due March 2004)