Wafer Level and Chip Size Direct Bonding at Room Temperature

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High temperature wafer bonding causes poor alignment between chip and substrate, gas formation in the hermetic cavities, and fracture across the bonded interface due to lattice mismatch of the materials. Room temperature bonding of multifunctional dissimilar materials can enhance the transmission of high-speed signal integrity, and reduce the size of optical and micro electromechanical systems (MEMS) devices. The article reports the wafer level and chip size bonding of Si, $LiNbO_3$, GaP, GaAs, and InAs using surface activated bonding process. The SAB can be defined as a fabrication process in which two solid surfaces are atomically cleaned by an energetic Argon ion, or fast atom beam in an ultra high vacuum (UHV) at room temperature. As a result, strong adhesion develops between atoms of the cleaned surfaces under intimate contact.

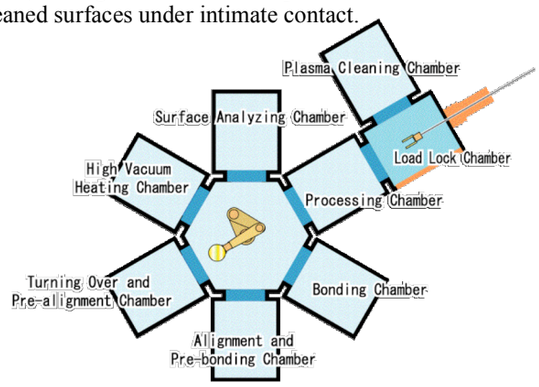

Figure 1. Schematic diagram of a wafer level bonding tool.

Fig. 1 shows the schematic diagram of the wafer level bonding tool which consists of a transfer chamber surrounded by a processing, a analyzing, a heating, a turning over/preliminary alignment, an alignment/preliminary bonding, and a bonding chambers. The SAB machine can accommodate up to 200 mm wafers. The pressure ranges from 10^{-5} to 10^{-6} Pa in all chambers. The wafer level samples (Si, $LiNbO_3$) were sputter cleaned in the processing chamber using a low energy Argon ion beam with a voltage of 80 V and an amperage of 3 A for 30-1800 s.

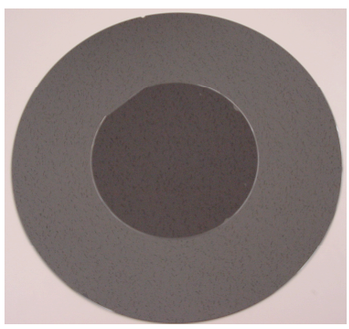

Figure 2. Infrared transmission image of 200mmSi/100 mm $LiNbO_3$ bonded at room temperature.

Bonding of $LiNbO_3$ with other semiconductors is of great interest for optical isolator because it has dual refraction modes. Fig. 2 shows the infrared image of 200 mm Si bonded with $LiNbO_3$ at room temperature. The wafers were bonded throughout the whole contact area. Tensile pulling tests showed a considerable homogeneity of bonding strength varied from 13 to 30 MPa for $Si/LiNbO_3$ and $LiNbO_3/LiNbO_3$. Microfliudic channels fabricated on 200 mm Si were successfully bonded with bare Si wafer (Fig. 3) for MEMS applications.

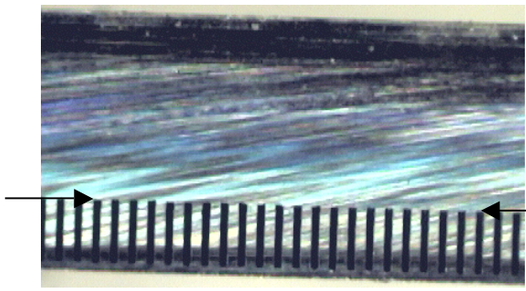

Fig. 3 shows the x-sectional SEM image for as-cut micro-cavities formed after bonding between bare Si and structured Si wafers. The thickness of the cavities was 180 μm. Arrows indicate the bonded interface.

For chip size bonding, the samples (Si, GaP, GaAs, and InaAs) were sputtered cleaned in the processing chamber of an UHV bonding tool (10^{-7} Pa) with a 1.5 kV Ar-FAB of dose rate of 2.38×10^{14} i/cm^{2}s for 30-60 s. Identical tensile results to that of wafer level were also obtained for chip size bonded samples (Fig. 5). We have fabricated Ohmic electrodes on both sides of the bonded samples and then measured the current-voltage behavior, which showed typical *p-n* junction with ideality factor nearly unity (Fig. 4). Additional results of atomic force microscope, and high-resolution transmission electron microscope observations for the surfaces and interfaces will be discussed.

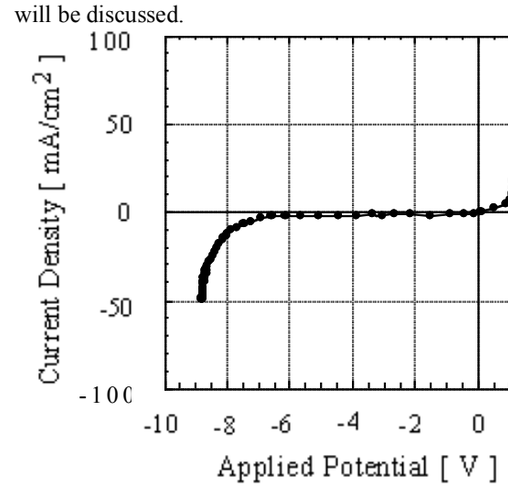

Figure 4. *I-V* characteristics of p-GaAs/n-GaP interface.

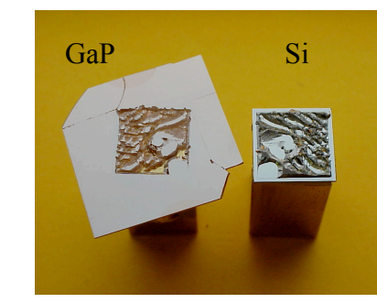

Fig. 5. Fracture images of chip size Si/GaP bonded at room temperature.