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Low loss optical fiber-chip interface for Silicon-on-Insulator nanophotonic integrated circuits.

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It is becoming more and more apparent that nanophotonic integration lies in the direct evolutionary path of current microelectronic technology. With the current advances in photo-lithography, circuit features are now substantially smaller than the relevant telecommunications optical wavelength of 440nm $\approx$ 1.55μm / n = λ/n, where n $\approx$ 3.5, is the refractive index of most common semiconductors.

To take advantage of the ever-progressing nano-fabrication technology we need to make correspondingly tiny optical devices. High degrees of optical miniaturization however, rely on the existence of high index contrasts: $\Delta n > 1$, which will allow devices to become much more compact than the core of an optical fiber. Such devices range from ring resonators to photonic crystal based devices such as nanocavities and waveguides.

Si/SiO_2 Silicon-on-Insulator (SOI) is one such high index contrast material system that has attracted a great deal of recent interest. Silicon is the material of choice of the electronics industry, and as such, processing techniques are well established. The superficial silicon of SOI presents us with a layer in which miniaturized optics and electronics could conceivably coexist in a high density optoelectronic IC. The vision is that of a hybrid nanophotonic /electronic circuit that would be completely compatible with CMOS fabrication technology.

Despite the integration advantages, the high index contrast system comes with a penalty. The need for single mode optical waveguides in the SOI nanophotonic ICs, requires that the waveguiding layer be approximately 200 nm thick. This results in a huge mode mismatch with single mode fiber, the core of which is roughly 50 X larger. This precludes the use of simple end-fire coupling to interface the optical fiber of the outside world with the nanophotonic circuit.

In this paper we describe a grating coupler based fiber-chip input/output interface that addresses this problem. The coupler is embedded in a specially designed high Δn dielectric stack in order to ensure high coupling efficiencies. We will discuss the design, CMOS compatible fabrication, and experimental demonstration of the coupler.

We will also describe other aspects of SOI nanophotonics research pursued in the Optoelectronics Group at UCLA.