Electric and thermal characteristics of multilayer thermionic power devices

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We analyze the performance of semiconductor multilayer thermionic power devices. The main bottleneck in the performance of the device is the conduction heat current, $\Delta T/R_{th}$ where ΔT is the temperature difference and R_{th} is the thermal resistance. Two mechanisms of reducing the heat backflow are proposed i) increasing R_{th} or ii) reducing ΔT. For bulk materials R_{th} can only be increased by a limited amount, dependent on the mean free path of carriers in the material. Even for InSb, the thermal resistance (per unit area) is still very small because of the device geometries required for ballistic transport. By introducing aperiodicity and specially designed interface boundaries in multilayer structures, the thermal resistance can be significantly reduced. In this work, we present several simulation results on the electrical and thermal characteristics of multilayer thermionic devices.