## Integration of Highly Ordered Carbon Nanotube Arrays onto Silicon Substrates A. J. Yin, L. Guo, K. Hanson, M. Tzolov, and J. M. Xu Division of Engineering, Brown University 182 Hope Street, Providence, RI 02912, USA

For many applications such as mechanical oscillators, displays and sensors, it is important to have uniform, aligned, and spatially and electrically separated nanotube arrays. We have previously shown that they can be easily and economically obtained via template synthesis using self-ordered anodic aluminum oxide (AAO) [1]. However, the earlier results were achieved using an aluminum (Al) foil as substrate, which is not always desirable and is difficult for integration with silicon (Si) based microelectronics. Recently, the formation of AAO using an evaporated or sputtered Al film on Si substrates has been studied, but attempts to grow highly ordered CNT arrays in the AAO on Si substrate have met with little success since thickness of the deposited Al is limited [2].

Here, we report two approaches for integrating ordered CNT arrays onto Si substrates. The first method is carried out by anodizing a thick Al film directly deposited on Si substrate using the conventional two step methods. High quality Al film was deposited in high vacuum  $(1 \times 10^{-8} \text{ Torr})$  via an e-beam evaporator, which was custom-designed with a temperature-controllable substrate heater and a rotating substrate-holding stage. The Al source is a high purity Al pellets (99.999%, COERAC). Different evaporation conditions, including the substrate temperature (up to 900K), evaporating rate and time, so as the Al thickness, were tested. Experimental results show that both substrate temperature and Al thickness are critical for the subsequent anodization to form highly ordered porous AAO films. From the trials, a set of optimal conditions emerged as follows: substrate temperature ~500K and thickness of Al film >40um. CNT growth was carried out by chemical vapor deposition (CVD) method in a tube furnace using C<sub>2</sub>H<sub>2</sub> or CH<sub>4</sub> as carbon source at temperature from 900K to 1200K. Fig. 1(a) and (b) show ordered and non-ordered CNTs on Si substrates from 40um and 10um thick Al films, respectively. Here, it's worth to mention that the barrier layer of AAO film on Si substrate can be removed, hence, the CNTs grown afterwards will have direct contact with the Si substrate resulting in a heterojunction structure, a good platform for photo-current generation.

The second method is a bonding technology. First, highly ordered CNT arrays (Fig.2) were grown on pure Al substrates, then, thin layers of gold were sputtered on both the CNT/Al sample and a Si substrate, finally, the CNT/Al chip was bonded onto the Si substrate via a thin layer of indium. To expose the CNT arrays from the alumina template, a wet-etching process, using a mixture of  $6\%H_3PO_4$  and  $1.8\%CrO_3$  with dispersant, was applied, where the added dispersant is critical for obtaining non-sticking exposed CNTs.

In conclusion, highly ordered CNT arrays on Si substrates can be obtained from direct anodization of thick Al films on Si substrates or by indium thermal bonding of CNT/Al chips onto Si substrates. These CNT arrays are good platforms for CNT property study and nanodevice development.

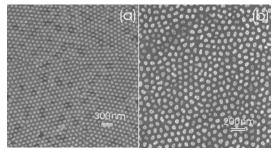


Fig. 1 SEM images show CNT arrays on Si substrates, from 40um (a), and 10um (b) Al films.

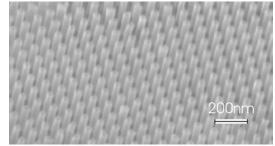


Fig. 2 SEM image shows exposed CNT array bonded on Si substrate after wet-etching

[1] J. Li, C. Papadopoulos, and J. M. Xu, Appl. Phys. Lett. 75, 367(1999)
[2] S. H. Jeong, K. H. Lee, Synth. Met. 139, 385(2003)