Novel Device Concepts for SiGe Nanoelectronics

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The goal of the ongoing research is the evaluation of an entirely new path to fabricate strained Si nano-devices which are compatible to Si CMOS processing. Two concepts basing on self assembled nanostructures will be introduced. The first idea - the disposable dot FET - is to fabricate field effect transistors from strained Si bridges, which have been manufactured by disposing embedded, sacrificial Ge islands (dots). This approach promises high speed electronics, due to the large mobility of carriers in

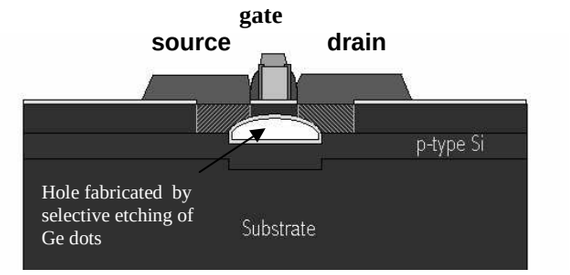

Fig.1 : Schematic illustration of the disposable dot FET

strained Si, substantially reduced short channel effects, since the thickness of the channel is defined by an air bridge, and an improved thermal conductivity, which is attributed to the all Si device design. To achieve the required positioning of the Ge dots, templated self assembling is explored using x-ray interference lithography (XIL) for the pre-pattern. It has been previously shown that pre-patterning of Si wafer by e-beam lithography to form very shallow lines (10-20 nm) can be successfully employed to align Ge dots along these shallow trenches.[1]. Molecular beam epitaxy as well as chemical vapour deposition is studied for the growth of the ordered Ge islands. To maximise the strain in the Si bridges Ge islands deposited at low temperature have to be overgrown in such a fashion that planarity is regained. First results on the pre-structuring using XIL, on low temperature growth of Ge dots, on their intermixing with Si analysed by in-situ STM and on the fabrication of strained Si bridges by selective etching of the Ge dots will be discussed.

The second idea follows the trail of FIN-FETs, but adding strained Si to it. The FIN is fabricated by carving a mesa line into a strained Si/SiGe bilayer placed on a scrificial layer. The removal of the sacrificial layer leads to scrolling of the strained bilayer into a ring, which can be layed down on the substrate surface using appropriate mesa design (Fig.2a). [2,3] Now the ring can act as a fin composed of vertical sheets of (partly) relaxed SiGe. and (partly) strained Si. At the outermost zone of the ring the SiGe will be almost completely relaxed. The Si at the inner surface of the ring is expected to be relaxed or even under compressive strain. Towards the center of the ring the Si will be under tensile strain whereas the Ge is under compressive strain. The amount of strain will depend on the Ge concentration in the SiGe film and on the exact location of the heterointerface within the ring, i.e. on the thickness of the SiGe and Si films of the bilayer, which can be adjusted accurately by epitaxial growth. Thus, these structures provide high mobility channels for electrons and holes.

To form the source and drain areas a second epitaxial step to grow those areas selectively might be necessary (Fig. 2b, left). However, depending on the bonding of the rings on the Si surface, it might be enough to place them across narrow Si grooves (Fig. 2b, centre). Thus the gate area of this “Ring-FIN-FET” can be formed. The gate length is defined by lithograph, whereas the width of the fin is given by the thickness of the epitaxial layers and the height of the fin by the width of the underetched mesa line. The advantages of this technology for FIN-FETs besides to the strained channels are the close to perfect sidewalls and the possibility to fabricate ultra-narrow fins without advanced lithography and etching techniques. In the paper, the fabrication technology for the rings will be discussed in detail. First results on the conductivity in scrolled Si/SiGe bilayers will be presented.

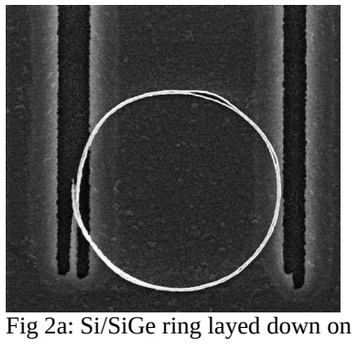

Fig 2a: Si/SiGe ring layed down on a Si (100) surface. The ring contains two turns, has a diameter of 2 µm and a wall width of 35 nm

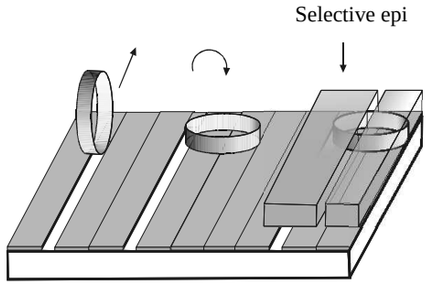

Fig. 2b: Schematic illustration of the formation of a “Ring-FIN-FET“

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