

Processing Challenges in the Fabrication of Advanced MEMS

A. Kornblit, V. A. Aksyuk, G. R. Bogart*, C. Bolle, J. E. Bower, R. A. Cirelli, E. Ferry, L. Fetter, A. Gasparyan, R. C. Keller, F. P. Klemens, W. Y.-C. Lai, O. D. Lopez, W. M. Mansfield, J. F. Miner, C.-S. Pai, F. Pardo, S. Pau, M. E. Simon, T. Sorsch, J. A. Taylor, D. M. Tennant and G. P. Watson

*Lucent Technologies Bell Labs
600 Mountain Ave., Murray Hill, NJ 07974*

As higher performance and complexity is demanded from advanced MEMS, the processes required to fabricate them are becoming much more demanding. Sub-micron features, rarely found in early MEMS, are now needed for improved performance, requiring the use of advanced lithography tools. Step and repeat cameras can deliver the required dimensions, but they are limited by their field size. When large area devices are needed, the repeated patterns can be tiled, thus enabling the realization of large MEMS with sub-micron features. In addition, the photoresist used by these advanced tools are sometimes too thin for the long dry etching steps, requiring the use of intermediate hard masks.

Deep silicon etching (or bulk micromachining) is challenging in terms of dimension, profile and uniformity control, and the realization of high etching rates. Fluorine based chemistries are commonly used to achieve high etching rates, and the profile is controlled either by relying on cryogenic or switched process. The latter, known also as the 'Bosch process,' relies on sequential etching and deposition steps, is the more common of the two. It is affected by loading, dimensional control is difficult and sidewalls tend to be somewhat rough, as a result of switching between etching and depositions steps. In addition, when a dielectric etch-stop layer is used (*e.g.*, in the

case of structures fabricated from SOI wafers), notching at the interface is a common occurrence.

Small dimension, high-aspect-ratio structures are common in advanced MEMS devices. In addition to patterning and etching these challenging structures, void-free deposition of dielectrics and polysilicon (and in some cases metal) is needed. There are numerous ways to deposit these films, which in many instances are sacrificial. Low pressure chemical vapor deposition (LPCVD), HDP oxide deposition or ozone TEOS are some of the processes that have been used in the past in the IC industry for gap-fill, and can be used for MEMS fabrication as well. In some cases these layers have to be flattened, requiring a challenging chemical-mechanical-polishing step, with high uniformity and little or no 'dishing.'

Since some of the structures contain cantilevers or mirrors that have to be flat, film stress control is an absolute must. Structures made of multiple films (*e.g.* silicon mirrors coated with metal) have to be flat not only after fabrication, but must remain flat after being placed in a system, and are expected to remain flat and function reliably for many years.

MEMS release is another challenging aspect of fabrication advanced MEMS, both in terms of avoiding stiction, and avoiding attack of metals that are present during the release process. A number of solutions, using both wet and dry chemistries are available for this process.

All of the above issues and ways to address them will be discussed.

* Current address: Sandia National Laboratories, Albuquerque, New Mexico