

TABLE OF CONTENTS

<i>Preface</i>	<i>iii</i>
<i>Conference organization</i>	<i>v</i>
Section I	1
Ultra-Shallow Junctions for Nanoscale CMOS	
1.* High Ramp Rate Rapid Thermal Annealing for Ultra-Shallow Junctions <i>P. Kohli, H.-J. Li, S. Ganguly, T. Kirichenko, B. Murto, E. Graetz, P. Zeitzoff, M. Pawlik, P.B. Merrill and S. Banerjee</i>	3
2. New Physics for Modeling Transient Enhanced Diffusion in RTP <i>M.Y.L. Jung, R. Gunawan, R.D. Braatz and E.G. Seebauer</i>	15
3.* Optical Effects in Diffusion and Activation Processes During RTA <i>R.B. Fair</i>	21
4. Spike Annealing for Ultra-Shallow Junction Formation <i>A. Jain</i>	33
5. Inherent Radiative Differences between Rapid Thermal and Furnace Annealing: Their Effects on Dopant Diffusion and Activation <i>P.S.-J. Choi and D.-L. Kwong</i>	41
6.* Ultra-Shallow Junction Formation Using Ion Implantation and Rapid Thermal Annealing: Physical and Practical Limits <i>A. Agarwal, H.-J.L. Gossmann, A.T. Fiory, V.C. Venezia and D.C. Jacobson</i>	49
7.* Role of Silicon and Boron Interstitial Clusters in Transient Enhanced Diffusion <i>N.E.B. Cowern, G. Mannino, F. Roozeboom, J.G.M. van Berkum, B. Colombeau and A. Claverie</i>	61
8. Ultra-Shallow P ⁺ -N Junctions for 35 – 70 nm CMOS using Selectively Deposited Very Heavily Boron-doped Silicon-Germanium Films <i>S. Gannavaram and M.C. Öztürk</i>	73
9.* Selective Epitaxial Si and SiGe for Elevated Source Drain MOSFETs <i>S.B. Samavedam, A. Dip, A.M. Phillips, J. Smith, J.M. Grant, W.J. Taylor and P.J. Tobin</i>	83
10.* Laser Thermal Processing (LTP) for Fabrication of Ultra-Shallow, Hyper-Abrupt, Highly Activated Junctions for Deca-Nanometer MOS Transistors <i>S. Talwar, Y. Wang, and C. Gelatos</i>	95
11.* Athermal Annealing of Silicon Implanted with Phosphorus and Arsenic <i>J. Grun, R.P. Fischer, M. Peckerar, C.L. Felix, B.C. Covington, D.W. Donnelly, B. Boro Djordjevic, R. Mignogna, J.R. Meyer, A. Ting, and C.K. Manka</i>	107

* *Invited paper*

12.* Exploring Alternative Annealing Methods for Shallow Junction Formation in Ion Implanted Silicon <i>K.S. Jones, H. Banisaukis, S. Earles, C. Lindfors, M. Griglione, M.E. Law, S. Talwar, S.W. Falk, D.F. Downey and A. Agarwal</i>	119
13.* Shallow Junction Challenges to Rapid Thermal Processing <i>L. Larson and B.C. Covington</i>	129
Section II Contacts for Nanoscale CMOS	137
14.* Aspects of Enhanced Titanium Salicide Formation <i>L. Kappius and R.T. Tung</i>	139
15. Multi-Substrate CoSi ₂ Formation Kinetics in a Low-Pressure, Susceptor-Based RTP Tool <i>A.J. Atanos, V. Parihar and S.-P. Sun</i>	151
16. Metal / Silicon Schottky Barrier Lowering by RTCVD Interface Passivation <i>Q.W. Ren, W.D. van Noort, L.K. Nanver and J.W. Slotboom</i>	161
Section III Gate Stacks for Nanoscale CMOS	167
17.* Ultrathin CVD Gate Dielectrics for 130 nm Technology Node <i>V.H.C. Watt, A. Karamcheti, T.-Y. Luo, H.N. Al-Shareef, M.D. Jackson and H.R. Huff</i>	169
18. High Performance, Highly Reliable Gate Oxide Formed with Rapid Thermal Oxidation In-Situ Steam Generation (ISSG) Technique <i>Y. Ma, Y.N. Chen, M.M. Brown, F. Li, Y. Chen, J. Eng, Jr., R.L. Opila, Y.J. Chabal, J. Sapjeta, D.A. Muller, G.C. Xing, T. Trowbridge, M. Khau and N. Tam</i>	179
19. High Reliable In Situ Steam Generation Process for 1.5-2.5 nm Gate Oxides <i>M. Bidaud, F. Guyader, F. Glowacki, F. Monsieur, D. Roy, S. Bruyère, E. Vincent and K. Barla</i>	187
20. Investigation of In-Situ Steam Generated Oxide (ISSG) followed by Remote Plasma Nitridation (RPN) for Effective Oxide Thickness Decrease and Gate Leakage Reduction <i>K. Eason, R. Jallepally, D. Noble, S. Hattangady, R. Khamankar and A.L.P. Rotondaro</i>	195
21.* Rapid Thermal Processing Using Steam <i>R. Sharangpani, J.H. Das and S.-P. Tay</i>	203
22. Corona-Charge Evaluation of Thermal SiO ₂ Growth by Single-Wafer and Batch Methods <i>A. Fiory, J. Zhang, P. Frisella, J. Hebb and A. Agarwal</i>	215

* *Invited paper*

23. Growth of Ultrathin Nitride on Si(100) by Rapid Thermal N ₂ Treatment <i>Z.H. Lu, A. Khoueir, W. T. Ng and S.-P. Tay</i>	223
24. Gate Dielectrics Formed by Remote Plasma Nitridation of Ultrathin In-Situ Steam Generated (ISSG) Oxides <i>H.N. Al-Shareef, T.Y. Luo, A. Karamcheti, G.A. Brown, M. Laughery, V.H.C. Watt, K. Torres, M.D. Jackson, H.R. Huff, K. Ahmed, R. Jallepally, D. Noble, N. Tam, and G. Miner</i>	231
25. In-situ Rapid Thermal N ₂ O Oxidation of NH ₃ -Nitrated Si for Ultrathin Nitride/Oxide Stack Gate Formation <i>Y.H. Kim, S.C. Song, H.F. Luan, J.C. Gelpey, A. Kepton, S. Levy, R. Bloom and D.-L. Kwong</i>	239
26. Processing and Characterization of RTCVD Silicon Nitride and Oxynitride Grown in a Single-Wafer RT Cluster Tool <i>C.P. D'Emic, E.P. Gusev, J. Newbury, P. Kozlowski, K. Chan, T. Zabel and P. Varekamp</i>	247
27.* Integrated Rapid Thermal CVD Oxynitride Gate Dielectric for Advanced CMOS Technology <i>H.-H. Tseng</i>	255
28. Ultrathin (EOT < 7 Å) Ta ₂ O ₅ Gate Stacks Prepared by an In-Situ RT-MOCVD Process <i>S.J. Lee, H.F. Luan, C.H. Lee, Y. Senzaki, D. Roberts and D.-L. Kwong</i>	263
29.* High-k Oxides by Atomic Layer Chemical Vapour Deposition <i>M. Tuominen, T. Kanninen and S. Haukka</i>	271
30. Electrical and Chemical Properties of Ultrathin RT-MOCVD Grown Ti-Doped Ta ₂ O ₅ <i>S.J. Lee, H.F. Luan, A. Mao, T.S. Jeon, C.H. Lee, R. Vrtis, D. Roberts and D.-L. Kwong</i>	283
31.* Electrical and Material Properties of Metal Silicate Dielectrics and Metal Gates for Advanced CMOS Devices <i>V. Misra, M. Kulkarni, G. Heuss, H. Zhong and H. Lazar</i>	291
32. RTCVD Polysilicon Grain Dimension Control <i>D. O'Meara, J. Conner, H.-H. Tseng, M. Rossow, T. Neil, V. Wang and C.-L. Chang</i>	299
Section IV	307
New Applications of RTP	
33.* Mechanisms and Applications of the Control of Dopant Profiles in Silicon Using Si _{1-x-y} Ge _x C _y Layers Grown by RTCVD <i>J.C. Sturm, M.S. Carroll, M. Yang, J. Gray and E. Stewart</i>	309

* *Invited paper*

34. High Performance Buried Silicon-Germanium Channel PMOST Fabricated Using Rapid Thermal Processing and Shallow Trench Isolation <i>D.J. Tweet, S.T. Hsu, D.R. Evans, B. Ulrich, Y. Ono and L. Stecker</i>	321
35. Kinetic Study of In-Situ Copper Oxidation and Reduction Using Rapid Thermal Processing and Its Applications in ULSI <i>Y.Z. Hu, R. Sharangpani and S.-P. Tay</i>	329
36. Development of an RTA Process for the Enhanced Crystallization of Amorphous Silicon Thin Films <i>Y.-G. Yoon, T.-K. Kim, K.-B. Kim, J.-Y. Choi, B.-I. Lee, and S.-K. Joo</i>	337
Section V	345
Advances in RTP Systems and Process Monitoring	
37. Optimization of Support Temperature in RTA-Tools by Scanning Infrared Depolarization Imaging of Monitor Wafers <i>H.-D. Geiler, H. Karge and B. Krimbacher</i>	347
38. Wafer Temperature Characterization During Low-Temperature Annealing <i>W.S. Yoo and T. Fukada</i>	355
39.* Determining the Uncertainty of Wafer Temperature Measurements Induced by Variations in the Optical Properties of Common Semiconductor Materials <i>B. Adams, A. Hunter, M. Yam and B. Peuse</i>	363
40. Low-Temperature Measurements and Monitors for Rapid Thermal Processing <i>P.J. Timans, N. Acharya and I. Amarilio</i>	375
41. In Situ Selectivity and Thickness Monitoring based on Quadrupole Mass Spectroscopy during Selective Silicon Epitaxy <i>E.A. Rying, G.L. Bilbro, M.C. Öztürk and J.C. Lu</i>	383
42. Optimization and Control of Gas Flows in an RTCVD Reactor <i>Y. Rainova, K. Antonenko, A. Barchotkin and J. Pezoldt</i>	393
43.* LEVITOR 4000: An Advanced RTP System Based on Conductive Heat Transfer <i>V.I. Kuznetsov, A.B. Storm, G.J. Snijders, C. de Ridder, T.A.M. Ruijl, J.C.G. van der Sanden and E.H.A. Granneman</i>	401
44. Ultra-Shallow Junction Formation of BF_2^+ Implants Using a Low-Pressure, Hot-Wall Rapid Thermal Anneal <i>V. Parihar, A.J. Atanos, K. Reddy and J.-F. Daviet</i>	413
45. Temperature Gradient Rapid Thermal Processor <i>J.-M. Dilhac and C. Ganibal</i>	421
46.* Spike Thermal Processing Using Arc-Lamps <i>D.M. Camm and M.E. Lefrançois</i>	429

* *Invited paper*

47. Novel High Ramp-Down Rate and Reflector Design in Rapid Thermal Processing <i>M.H. Lee and C.W. Liu</i>	437
48. Improved Performance of a Fast-Ramp RTA System through Recipe and Controller Optimization <i>S. Ramamurthy, A. Mayur, D. de Roover, and J.L. Ebert</i>	445
Section VI Author Index and Key Word Index	453
Author Index	455
Key Word Index	459