

## TABLE OF CONTENTS

<i>PREFACE</i>	v
<b>ELECTRONICS DIVISION AWARD ADDRESS</b>	
Radical Reaction Based Semiconductor Manufacturing for Very Advanced ULSI Process Integration* T. Ohmi	3
<b>KEYNOTE PAPERS</b>	
From Ambient Intelligence to Silicon Process Technology * C.J. van der Poel	7
From the Lab to the Fab: Transistors to Integrated Circuits * H. R. Huff	15
Diffused Silicon Transistors and Switches (1954-1955): The Beginning of Integrated Circuit Technology * N. Holonyak Jr.	68
Current Status and Future Prospects in Mixed Signal SOC * A. Matsuzawa	107
<b>PROCESS INTEGRATION FOR MEMORY DEVICES</b>	
DRAM Technology for 100nm and Beyond * K.H. Küsters, J. Alsmeier, J. Faul, J. Lützen and T. Zell	123
Logic Based Embedded DRAM Technologies* C. Mallardeau	133
Flash Memory Technology Evolution* R. Bez and E. Camerlenghi	136
FeRAM Technology: Today and Future * I. Kunishima and N. Nagel	149
Effects of Nitridation Treatment for Electrochemical Properties of MONOS Non-Volatile Memories H. Aozasa , I. Fujiwara, K. Nomoto, H. Komatsu and T. Kobayashi	152
The Crystallization Behavior and Interfacial Reaction of Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> Thin Films Between Dielectric Material for the Application to the Phase Change Memory E.J. Jung, S.K. Kang, B.G. Min and D.H. Ko	159
* Invited paper	

## FULL PROCESS INTEGRATION ASPECTS

Single-Wafer Technology in a 300-mm Wafer Fab* S. Ikeda, K. Nemoto and M. Funabashi	163
The Impact of Single Wafer Processing on Process Integration* R. Singh, M. Fakhruddin and K.F. Poole	171
Advanced Multilevel Interconnects Technologies for 40-nm Lg Devices* T. Ohba	183
Performance Limitations of Metal Interconnects and Possible Alternatives* K.C. Saraswat, P. Kapur and S. Souri	194
Plasma Technologies for Low-k Dry Etching* T. Tatsumi	206
A Novel Approach to Contact Integration at 90-nm and Beyond A. Singhal, T. Sparks, K. Strozewski, F. Huang, S. Parihar, J. Schmidt, B. Boeck, J. Fretwell, G. Yeap, V. Sheth, S. Veeraghavan and B. Melnick	217

## SiGe PROCESS INTEGRATION

BiCMOS Integration of High-Speed SiGe:C HBTs* H. Rücker, B. Heinemann, R. Barth, D. Knoll, D. Schmidt and W. Winkler	223
Applications of Silicon Germanium Electrodes in ULSI * E.-X. Ping, E. Blomiley and F. González	230
Noise Properties and Hetero-Interface Traps in SiGe-Channel PMOSFETs* T. Tsuchiya and J. Murota	241
Ultra-Shallow Junction Formation by Low Energy Ion Implantation and Flash Lamp Annealing* K. Suguro, T. Ito, T. Itani and T. Iinuma	253

## INTEGRATION ASPECTS FOR EMERGING TECHNOLOGIES

Single and Few Electron Devices. Integration Trends* J. Gautier	263
Achieving Low Junction Capacitance on Bulk Si MOSFET Using SDOI Process* Z. Wang, T. Abbott, J. Trivedi, C.-C. Cho and M. Violette	266

\* Invited paper

Differential Silicide Thickness for ULSI Scaling*	278
W.J. Taylor Jr., J. Smith, J.-Y. Nguyen, R. Rai, O. Adetutu, J. Geren, J. Ybarra and D. Petru	
High-Voltage CMOS and Scaling Trends*	288
H. Ballan	
Emerging Device Solutions for the Post-Classical CMOS Era*	291
K. De Meyer, N. Collaert, S. Kubicek, A. Kottontharayil, H. van Meer and P. Verheyen	
Modeling End-of-the-Roadmap Transistors*	306
A. Asenov, A.R. Brown and J.R. Watling	
Thin Film Transistors in ULSI –Status and Future*	322
Y. Kuo	
Extending Planar Single-Gate CMOS & Accelerating the Realization of Double-Gate/Multi-Gate CMOS Devices*	330
J.O. Borland, H. Iwai, W. Maszara and H. Wang	

### **SURFACE PREPARATION AND GATE MODULE**

Cleaning for Sub 0.1 $\mu\text{m}$ Technology: A Particular Challenge*	349
D.M. Knotter	
Si Channel Surface Dependence of Electrical Characteristics in Ultra-Thin Gate Oxide CMOS*	361
H.S. Momose	
Integration Issues with High k Gate Stacks*	375
C.M. Osburn, S.K. Han, I. Kim, S.A. Campbell, E. Garfunkel, T. Gustafson, J. Hauser, T.-J. King, Q. Liu, P. Ranade, A. Kingon, D.-L. Kwong, S.J. Lee, C.H. Lee, J. Lee, K. Onishi, C.S. Kang, R. Choi, H. Cho, R. Nich, G. Lucovsky, J.G. Hong, T.P. Ma, W. Zhu, Z. Luo, J.P. Maria, D. Wicaksana, V. Misra, J.J. Lee, Y.S. Suh, Z. Luo, G. Parksons, D. Niu and S. Stemmer	
Compatibility of Polysilicon with $\text{HfO}_2$ -based Gate Dielectrics for CMOS Applications	391
V. Kaushik, S. De Gendt, M. Caymax, E. Young, E. Rohr, S. Van Elshocht, A. Delabie, M. Claes, X. Shi, J. Chen, R. Carter, T. Conard, W. Vandervorst, M. Schaekers and M. Heyns	
Analysis of CMOS Gate-To-Drain Leakage Current and Proposition of a New Cobalt Salicide Selective Etch Chemistry for High DRAM Yield	397
B. Froment, C. Régnier and M.-T. Basso	

\* Invited paper

Electrical Characteristics and Thermal Stability of $W_2N/Ta_2O_5/Si$ MOS Capacitors in $N_2:H_2$ or $H_2$ Ambients P.C. Jiang and J.S. Chen	400
Sub-Quarter Micron PMOSFET DC and AC NBTI Degradation E. Li, S. Prasad, S. Park and J. Walker	408
<b>PROCESS INTEGRATION IN INTEGRATED CIRCUIT APPLICATIONS</b>	
Physical Analysis and Modeling of Plasma Etching Mechanism for ULSI Application* M. Kanoh, S. Onoue, K. Nishitani, T. Shinmura, K. Iyanagi, S. Kinoshita and S. Takagi	421
Process Strategy for Built-in Reliability of Cu Damascene Interconnect System for 0.13 $\mu$ m-Node and Beyond * H. Yamaguchi, T. Oshima, J. Noguchi, K. Ishikawa, H. Aoki, T. Saito, T. Furusawa and K. Hinode	434
Impact of Wafer Backside Cu Contamination to 0.18 $\mu$ m Node Devices S.Q. Gu, L. Duong, J. Elmer and S. Prasad	447
Integrated Multiscale Process Simulation of Damascene Structures M.O. Bloomfield, Y.H. Im, J. Seok, C.P. Sukam, J.A. Tichy and T.S. Cale	455
An Analysis of the Effect of the Steps for Isolation Formation on STI Process Integration A. Pavan, D. Brazzelli, M. Aiello, C. Capolupo, C. Clementi, C. Cremonesi and A. Ghetti	467
Defect Generation and Suppression in Device Processes Using a Shallow Trench Isolation Scheme D. Peschiarolli, M. Brambilla, G.P. Carnevale, A. Cascella, F. Cazzaniga, c. Clementi, C. Cremonesi, A. Gilardini, M. Martinelli, A. Maurelli, I. Mica, A. Pavan, G. Pavia, F. Piazza, M.L. Polignano, V. Soncini and E. Bonera	477
Electrodeposition of Low-Dimensional Phases on Au Studied by EQCM and XRD C. Shannon	489

\* Invited paper

## SILICON-ON-INSULATOR

60-nm Gate Length SOI CMOS Technology Optimized for “System-on-a-SOI-Chip” Solution*	493
K. Imai, S. Maruyama, T. Suzuki, T. Kudo, S. Miyake, M. Ikeda, T. Abe, S. Masuda, A. Tanabe, J.-W. Lee, K. Shibahara, S. Yokoyama and H. Ooka	
Emerging Silicon-On-Nothing (SON) Devices Technology*	503
T. Skotnicki, S. Monfray and C. Frenouillet-Beranger	
	518
High Performance Strained-SOI CMOSFETs*	
S.-I. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, Y. Moriyama, S. Nakaharai, J. Koga, A. Tanabe and T. Maeda	
Extremely Scaled Ultra-Thin Body and FinFET CMOS Devices*	534
S. Balasubramanion, L. Chang, Y.-K. Choi, D. Ha, J. Lee, P. Ranade, S. Xiong, J. Bokor, C. Hu and T.-J. King	
Fully Depleted SOI Process and Device Technology for Digital and RF Applications*	546
F. Ichikawa, Y. Nagatomo, Y. Katakura, S. Itoh, H. Matsushashi, N. Hirashita and S. Baba	
Status and Future Development of PDSOI MOSFETs*	556
S. Krishnan	
Multi-fin Double Gate MOSFET Fabricated by Using (110)-Oriented SOI Wafers and Orientation dependent Etching	566
Y.X. Liu, K. Ishii, T. Tsutsumi, M. Masahara, H. Takashima and E. Suzuki	
Optimization of Ultra-Thin Body, Fully-Depleted-SOI Device, with Raised Source/Drain or Raised Extension	572
J.L. Egley, A. Vandooren, B. Winstead, E. Verret, B. White and B.-Y. Nguyen	
Partially Depleted SOI Dynamic Threshold MOSFET for Low-Voltage and Microwave Applications	578
M. Dehan, D. Vanhoenacker-Janvier and J.-P. Raskin	
New Characterization Techniques for SOI and Related Devices*	584
S. Okhonin, M. Nagoga and P. Fazan	
Authors Index	587
Subject Index	591

\* Invited paper