# From Bell Labs to Silicon Valley: A Saga of Semiconductor Technology Transfer, 1955-61\*

#### by Michael Riordan

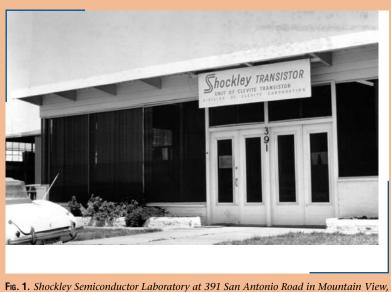
espite the fact that the Bell Telephone Laboratories had originated almost all the silicon technology eventually used to invent the integrated circuit, or microchip, this revolutionary breakthrough occurred elsewhere-at Texas Instruments, Inc., in Dallas, and Fairchild Semiconductor Corporation in Mountain View, California. In the latter case, the transfer of this technology occurred largely through the offices of a pivotal but ultimately unsuccessful company, Shockley Semiconductor Laboratory, which had been formed by transistor pioneer William Shockley. After leaving Bell Labs in 1955, he brought together a stellar team of scientists and engineers who later departed (in September 1957) to found Fairchild, bringing a deep understanding of the diffused-silicon technologies they had learned while employed by Shockley.

One pivotal contribution to silicon technology, however, originated entirely at Fairchild—the planar manufacturing process invented and developed by the physicist Jean Hoerni. This crucial technique, in which an oxide layer on the silicon surface is used to protect the sensitive *p*-*n* junctions beneath it, has served ever since 1961 as the basis of microchip fabrication. And Hoerni's conception of this method occurred substantially earlier than most historical accounts have thus far reported.

In this article, I try to set the record straight by recounting the important steps and major influences that brought silicon technology to California—in the process laying the technological foundations of Silicon Valley.

# **Silicon Technology Heads West**

By 1954 William Shockley was becoming increasingly frustrated by his lack of professional advancement at Bell Labs. Although head of transistor research, he had been passed over for higher positions and seemed mired at this middle-management level despite his many publications and patents, including the all-important ones on the junction transistor. Thus he began casting around for other possible positions, taking a leave of absence to serve as a visiting professor at Caltech and as a military advisor in the Pentagon's Weapons Systems Evaluation Group. But neither option



**Fig. 1.** Shockley Semiconductor Laboratory at 391 San Antonio Road in Mountain View, California, as it appeared in 1960 after Clevite Corporation had purchased it and renamed it Shockley Transistor Company. (Courtesy of Kurt Hübner)

proved satisfying. So by early 1955 Shockley was seeking to get back into industrial research—this time as the head of his own company.<sup>1</sup>

In March 1955 his sense of urgency in these efforts was stimulated by news from Bell Labs. Not only had chemist Henry Theurer finally produced silicon with impurity levels of less than a part per billion using float-zone refining. But Morris Tanenbaum and D. E. Thomas had also succeeded in forming the first diffused-base (and emitter) silicon transistor using samples provided by Calvin Fuller (see article by Nick Holonyak on p. 30). "Morrie Tann has AlSb plus Al bonded," reads a cryptic note in Shockley's pocket notebook dated 23 March 1955, while he was still at the Pentagon, referring to micrometers-thin aluminum and antimony impurity layers diffused into the silicon.<sup>2</sup>

Over the next few months, Shockley began talking with executives at RCA, Raytheon, Texas Instruments and elsewhere about the possibility of starting a firm expressly devoted to producing diffused-silicon devices. For most of that summer, he met with only passing interest until he spoke with his friend and fellow Caltech alumnus Arnold Beckman, founder and president of Beckman Industries, Inc. In early September they met in Newport Beach, California, and agreed to found a new division led by Shockley whose purposes included "the development of automatic means for production of diffused-base transistors."<sup>3</sup>

His original plan was to lure away some of his most accomplished Bell Labs colleagues, such as Tanenbaum and Morgan Sparks, who had fabricated the first junction transistors. But one by one they turned him down that fall, claiming their families were too deeply rooted in New Jersey and they could not bear to leave Bell Labs. Thus he subsequently criss-crossed the United States, trying to recruit the best possible scientists and engineers for Shockley Semiconductor Laboratory. And he hired some top-notch ones, too: physicists Hoerni from Caltech, Jay Last from MIT, and Robert Noyce from Philco-as well as physical chemist Gordon Moore from the Johns Hopkins Applied Physics Laboratory. Among the eldest of this group at age 28, Noyce was about the only one with extensive semiconductor experience, having developed highfrequency germanium transistors at Philco.4

Only Noyce among them had attended the third Bell Labs symposium on transistor technology in January 1956, devoted to the advanced silicon technologies just then being developed—especially diffusion. But because Beckman had licensed the rights to the transistor patents from Bell's parent company, AT&T, Shockley and his new employees had ready access to the information presented there, including early preprints of the papers that

\* Adapted in part from *Crystal Fire: The Birth of the Information Age,* by Michael Riordan and Lillian Hoddeson, W. W. Norton & Co., New York (1997), esp. pp. 225-275. See also M. Riordan and L. Hoddeson, "The Moses of Silicon Valley," *Physics Today*, pp. 42-47 (December 1997).



**FIG. 2.** Senior staff of Shockley Semiconductor Laboratory toast their illustrious leader William Shockley (seated at head of table) at a celebratory luncheon on 2 November 1956, the day after the announcement of his Nobel Prize. Seated at left is Gordon Moore and right of him is Sheldon Roberts. Robert Noyce stands in the middle and Jay Last is at far right, both lifting glasses. (Courtesy of Intel Corporation)

would be published in 1958 as the final volume in the classic series, Transistor Technology, which was becoming known throughout the semiconductor industry as "Ma Bell's cookbook."5 Shockley could also call upon his old colleagues Sparks, Tanenbaum, and Jack Morton, head of device development, to visit the new California company and consult with his charges in their converted Quonset hut at 391 San Antonio Road (Fig. 1). They spent most of that first year purchasing or building the necessary equipment, such as silicon crystal growers and diffusion furnaces, and learning how to use it in making semiconductor devices.

On 1 November 1956, marvelous news reached the Mountain View firm that Shockley had won the 1956 Nobel Prize in physics for the invention of the transistor, shared with John Bardeen and Walter Brattain. The next day they stopped working before noon for a celebratory luncheon at nearby Rickey's Studio Inn in Palo Alto. A photograph of that gathering (Fig. 2), with Shockley at the head of the table being toasted by Noyce, Moore, Last, and others around him, has achieved iconic status in the lore of Silicon Valley.<sup>6</sup>

Upon returning from Stockholm in mid-December, Shockley found a package in his mail from the patent licensing engineer at Western Electric Company, AT&T's manufacturing arm. It contained a preprint of an article by Carl Frosch and Lincoln Derick titled "Surface Protection and Surface Masking during Diffusion in Silicon." Frosch had delivered a paper on diffusion in the third transistor symposium, but it did not contain much information about use of a silicon-dioxide layer to passivate the silicon surface because Bell Labs was still applying for a patent on this important method. The preprint also contained crucial new information about how to etch tiny openings in that layer and to use the remaining oxide as a mask against the diffusion of trace impurities into the silicon. That technique would allow workers to establish intricate patterns of n-type and *p*-type material in the silicon. Shockley circulated this document among his technical staff (Fig. 3), giving them all a crucial early glimpse of what would become one of the core enabling technologies for silicon integrated circuits and ultimately lead to the emergence of Silicon Valley.7 By the time Frosch and Derick's paper was published in the Journal of The Electrochemical Society the following September, Shockley and his staff were already developing ways to implement this disruptive new technology.8

## A Rebellion Erupts

But all was not well at the Mountain View laboratory. By 1957, members of the technical staff had begun to resent Shockley's often heavy-handed management style and his quirky selection of R&D projects. After a couple of worrisome incidents, he started investigating the backgrounds of a few of his employees. And he gave one of them a vicious, embarrassing tongue-lashing that many others overheard. Several of the early employees were extremely dissatisfied and ready to quit.<sup>9</sup>

For reasons about which we can only guess, Shockley had lost interest in the original goal set for the firm—manufacturing diffusedbase transistors. He instead began

to focus the company's talents and energies on devices that were then at the frontiers of semiconductor technology, such as field-effect transistors and the four-layer p-n-p-n diode, often called the Shockley diode because he held a patent on it. At a given potential called the breakdown voltage, current would suddenly begin to flow through the two-terminal device, switching it from "off" to "on." A remarkably simple, compact semiconductor switch, it was the ultimate realization of a goal that had been subtly implanted in Shockley's mind at Bell Labs two decades earlier.<sup>10</sup>

Although a brilliant conception, however, the four-layer diode was extremely difficult to fabricate with uniformity and reliability. Workers had to polish a silicon wafer to have exactingly parallel planes on its two sides and then carefully diffuse impurities into the wafer from both sides simultaneously. Lack of enough precision meant the diffused impurities would penetrate to irregular, unpredictable depths, leading to variations in the breakdown voltage and other electrical characteristics.<sup>11</sup>

Noyce, Moore, and others thought that this diode was much too difficult a project for the young company to attempt at such an early stage in its evolution. We should concentrate

Naund DEC 2 4 1956 6 Western Electric Company 195 BROADWAY NEW YORK 7. N.Y. December 14, 1956 DUCTOR LABORATORY OF TTS, INC. 10 Road So. San Antonio Road tain View, California Shockley: Enclosed is a copy of a paper entitle re Frotection and Selective Masking Duris ion in Silicon", by Messrs. C. J. Frosch ick of the Bell Telephone Laboratories. entitled. I trust that this article will be of value to you in your semiconductor work. Very truly yours, A. T. DAVID Patent License Engineer Please route Julius Blank A In Tak del Victor Grinish UN William Happ #-Jean Hoggiff

**FIG. 3.** Copy of the 14 December 1956 letter to Shockley from the Western Electric patent engineer that accompanied a preprint of Frosch and Derick's paper on oxide masking, plus the initialed routing list of technical staff members of Shockley Semiconductor Laboratory who read this paper. (Stanford University Archives)

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first on three-layer devices such as the diffused-base transistor, they argued, and get a product out the door. After that they could begin attempting the more difficult problem of fabricating the four-layer diode. But Shockley was not listening and began devoting more and more of the company's resources to this pet project. He eventually set up a separate R&D group working mostly in secret on the four-layer diode, which further angered technical staff members left out of the loop.

The conflict reached the boiling point in mid-May 1957, when Beckman came up for a meeting to discuss the division's problems and plans. Taking umbrage at his partner's proposals and request to control expenses, however, Shockley stood up and stomped out of the room, shouting, "If you don't like what we're doing here, I can take this group and get support any place else!"<sup>12</sup>

But nobody left the room except Shockley. His outburst triggered a fourmonth sequence of events that led in September to the departure of eight of his top lieutenants—including Hoerni, Last, Moore, and Noyce. A pivotal moment in the history of the semiconductor industry, it is briefly recorded in yet another Shockley notebook: *"Wed 18 Sep—Group resigns."*<sup>13</sup>

## A Successful Semiconductor Company

Within days the group of eight rebels—which also included the metallurgist Sheldon Roberts and engineers Julius Blank, Victor Grinich, and Eugene Kleiner-signed a \$1.38 million agreement brokered by the investmentbanking firm Hayden Stone with Fairchild Camera and Instrument Corporation of Syosset, New York, on Long Island (Fig. 4). Using these start-up funds, the eight began setting up a new firm known as the Fairchild Semiconductor Corporation just over a mile away on Charleston Street in Palo Alto.14

At almost exactly the same moment, Frosch and Derick's revolutionary paper was published in the September 1957 issue of the *Journal of The Electrochemical Society*. But because they had read the preprint of this paper while working at Shockley Lab, the Fairchild upstarts had a big head start on most of the competition. According to Roberts, some of them—including Hoerni, Moore, and Noyce—had already begun experimenting with double diffusion and oxide masking while they were there.<sup>15</sup>

The first commercial product attempted by Fairchild was a highfrequency, diffused-base silicon transistor to drive core memory in an onboard computer that IBM was making for the guidance-and-control system of the B-70 bomber. The eight partners began applying the silicon technology they had learned and developed at Shockley Semiconductor. Roberts grew silicon crystals while Moore tackled issues of diffusing impurities into them. Last and Noyce took on the intricate tasks involved in oxide masking and photolithography, developing a "step-and-repeat" camera to aid them in defining tiny, precise *n*-type and *p*-type areas in the silicon wafers.<sup>16</sup>

By May 1958 the group had successfully fabricated prototype *n-p-n* silicon transistors, based on the "mesa" structure pioneered by Tanenbaum and Thomas at Bell Labs.<sup>17</sup> In such a structure, a thin *p*-type base layer and an *n*-type emitter layer were diffused into an *n*-type silicon wafer that formed the collector of this bipolar junction transistor. Oxide masking and photolithography were used

staff members remaining at Shockley Semiconductor Laboratory were still struggling to make four-layer diodes.

## The Planar Manufacturing Process

But a serious problem emerged with these mesa transistors that threatened the continued success of the fledgling company. Some of these devices experienced catastrophic failures that were traced to bits of foreign material being dislodged and becoming attached to the exposed junctions, attracted by strong electric fields there. Merely tapping on the metal cans housing these transistors with a pencil eraser was often sufficient to trigger such failures.



**FIG. 4.** Official photograph (circa 1960) of the eight Fairchild founders, who later became famous in Silicon Valley lore as the "Fairchild Eight." Left to right, Gordon Moore, Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni, and Jay Last. (Wayne Miller photograph courtesy of Fairchild Semiconductor Corp. and Magnum Photos)

to define these regions. But after attaching the electrical leads, workers etched away any remaining portions of the silicondioxide sheath, exposing the underlying junctions. This was standard practice in the semiconductor industry at the time, for the oxide layer was widely viewed as "dirty"—especially at Bell Labs.

Fairchild's transistors were the first commercially successful mesa transistors, beating out Texas Instruments, which was also working on similar devices. Not only did they meet IBM's stringent specifications, but they also began to be used in other avionics applications. Fairchild Semiconductor recorded sales of over \$500,000 —almost all of it coming from this product—in 1958, its first full year of operations, and ended the year in the black.<sup>18</sup> Meanwhile, the loyal This was a fundamental design flaw of the exposed mesa structure. A possible solution being considered was to try to leave the oxide layer in place over the junctions—or deliberately form one there in order to protect them during the final processing steps.<sup>19</sup>

A far more elegant approach was put forth by Jean Hoerni, who had been leading Fairchild's efforts to fabricate *p*-*np* transistors to satisfy IBM's specifications. A theoretical physicist by training, Swiss-born Hoerni had earned advanced degrees from the Universities of Geneva and Cambridge, and often worked on his own. At Shockley Lab he at first had an office separate from the Quonset hut, where he could go off by himself to calculate diffusion curves and other useful theoretical quantities.<sup>20</sup>

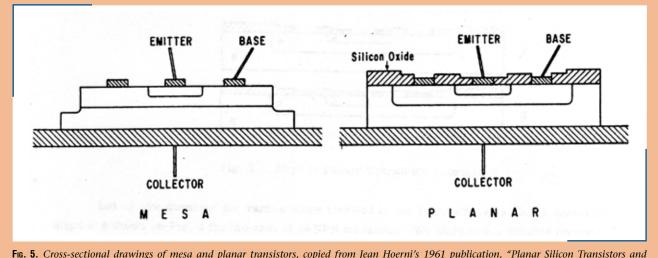


Fig. 5. Cross-sectional drawings of mesa and planar transistors, copied from Jean Hoerni's 1961 publication, "Planar Silicon Transistors and Diodes," Fairchild Semiconductor Corp. Report No. TP-14. (Stanford University Archives)

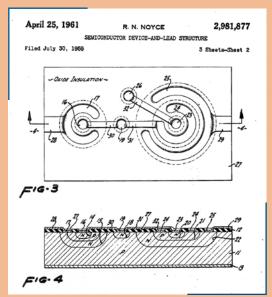
While the Fairchild founders were busy setting up offices and equipment on Charleston Street, Hoerni had already begun to consider a new and different way to fabricate transistors. An admitted contrarian, he suggested that instead of etching away the oxide layer at the end of processing, it instead be *left in place* to protect the sensitive junctions. He entered this revolutionary new idea on pages 3 and 4 of his crisp new lab notebook on 1 December 1957, hardly more than *two months* after the firm had been founded!<sup>21</sup>

Titled "Method of protecting exposed *p-n* junctions at the surface of silicon transistors by oxide masking techniques," it was witnessed that same day by Noyce. The very first paragraph is revealing:

The general idea underlying this invention is the building up of an oxide layer prior to diffusion of dopant atoms at the places on the surface of the transistor at which p*n* junctions are expected to emerge from the body of the semiconductor. The oxide layer so obtained is an integrant (sic) part of the device and will protect the otherwise exposed junctions from contamination and possible electrical leakage due to subsequent handling, cleaning, [and] canning of the device.2

This approach had the further advantages that all electrical leads could be attached and all processing steps performed from the *same side* of the silicon wafer—features that would eventually prove to be of inestimable value when this planar manufacturing process was later applied to fabricating integrated circuits. With only slight exaggeration, historian of technology Christophe Lécuyer has called this planar process "the most important innovation in the history of the semiconductor industry."<sup>23</sup>

When Hoerni conceived this approach in December 1957, Fairchild lacked the technical abilities needed to implement it. And the new firm's talents and energies had to be devoted almost entirely to getting its first mesa transistors out the door. But once the techniques of diffusion, oxide masking photolithography had been and mastered in 1958, he returned to his conception as a way to address their reliability problems. With the help of Last, who made the extra mask he needed, Hoerni proved out this idea in March 1959, fabricating prototype planar transistors that avoided the problems of



**FIG. 6.** Drawings from Robert Noyce's patent on the integrated circuit, showing how he proposed to use Hoerni's planar processing technique to form the necessary p-n junctions in silicon beneath a protective oxide layer. Silicon is denoted by 11 here and silicon dioxide by 12.

the failure-prone mesas (Fig. 5). What's more, he soon showed they had far superior electrical characteristics—with higher gains, and leakage currents often less than a nanoampere. As Hoerni concluded in a paper that he presented at an October 1960 meeting on electron devices in Washington, DC, "the planar design offers considerable improvement and stabilization of the parameters most likely to suffer from surface contamination."<sup>24</sup>

On 14 January 1959, Hoerni had had a Fairchild secretary type up a formal patent disclosure to give the company's attorney. Apart from a few typographical changes and improved drawings, it is *completely identical* to the 1 December 1957 entry in his lab

notebook—indicating the great accuracy of his original theoretical insight.<sup>25</sup> Just a few months later Moore and Noyce, who had by then emerged as the natural leaders of the new firm, decided to reorient Fairchild's transistor production lines to this promising new planar approach.<sup>26</sup>

## The Monolithic Idea Becomes Reality

Only nine days after Hoerni's formal patent disclosure, Noyce, stimulated in part by the urgings of the patent attorney, began writing in his lab notebook under the heading, "Method of isolating multiple devices."27 He thought it a terrible waste that all these transistors on a single wafer had to be cut apart, have leads attached to them individually, and then be soldered back together with other components to assemble complete circuits. What if all the interconnections could be instead placed directly on the wafer surface during the manufacturing process? Here again, the silicon-dioxide

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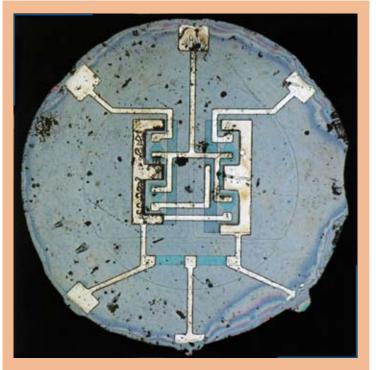
layer played the key role as an enabling technology.

"In many applications now it would be desirable to make multiple devices on a single piece of silicon in order to be able to make interconnections between devices as part of the manufacturing process, and thus reduce size, weight, etc., as well as cost per active element, Noyce began.<sup>28</sup> To Hoerni's planar process, he added the provision that aluminum interconnections between the individual devices be placed on top of the oxide layer, which would insulate these leads from the silicon beneath it. And these circuit components could be electrically isolated from one another by interposing back-to-back p*n* junctions between them. These were the principal new ideas at the heart of Noyce's famous integrated-circuit patent, titled "Semiconductor Deviceand-Lead Structure," which he applied for later that year (Fig. 6).29

The difficult task of actually fabricating microelectronic circuits according to these prescriptions fell to Jay Last, who formed a development group to realize this goal. In March 1959 Noyce took over as Fairchild's General Manager and Moore replaced him as research director. Noyce rarely showed up in the laboratory after that—and then only to check up on how work was progressing.<sup>30</sup>

Production of planar transistors was proceeding apace in 1959, especially at the urging of Autonetics, a division of North American Aviation that was building computer systems for the Minuteman missile and had extremely stringent demands for precision and reliability. It helped Fairchild to learn that a Bell Labs group under M. M. Atalla had developed "thermal" methods of growing the oxide, mitigating the problems of dangling bonds and "surface states" at the interface between the oxide layer and the silicon.<sup>31</sup> Using this thermally grown oxide layer, Atalla and Dawon Khang subsequently made the first truly successful fieldeffect transistors in 1960-what soon became known as the metal-oxidesemiconductor, or MOS, transistor (see article by Ross Bassett on p. 46).<sup>32</sup>

It took Last's development team nearly two years to produce commercially available integrated circuits using planar processing. Higher precision was needed for oxide masking and photolithography—and more steps were involved. And a big problem was isolating the circuit elements. Workers even attempted a physical-isolation approach suggested by Last that involved etching channels between the components from the back of the wafer all the way to the fragile oxide layer, then filling these



**FIG. 7.** One of the earliest prototype integrated circuits fabricated by Jay Last's development group at Fairchild using the planar processing technique. This "flip-flop" logic circuit employed four transistors. (Courtesy of Fairchild Semiconductor Corp.)

channels with an inert epoxy resin. But in the fall of 1960, *p-n* junction isolation proved the superior alternative. The group made successful prototype flipflop circuits involving four transistors (Fig. 7) and followed them up with other integrated logic circuits. In March 1961 Fairchild announced the "Micrologic" family of integrated circuits, half a year ahead of the Texas Instruments competition. The use of Hoerni's planar processing technique had made all the difference.<sup>33</sup>

#### Summary

Throughout this technological evolution, from diffused-base transistors to planar integrated circuits, the silicon-dioxide layer discovered in 1955 by Frosch and Derick remained at the center of the action. Without this supple, flexible interface between silicon and its environment, the microchip as we know it today would be unthinkable. It is the *sine qua non* of the semiconductor industry, and what most distinguishes silicon from all other material alternatives.

Although ultimately unsuccessful financially, the Shockley Semiconductor Laboratory played an important technology-transfer role in this saga. It acted as the crucial incubator where men came together with ideas on the West Coast, and began working together on the revolutionary implications of the new silicon technologies pioneered in the mid-1950s by Bell Labs. They were so revolutionary, in fact, that it took a small rebellion, much celebrated in Silicon Valley lore, to realize them. The development and implementation of planar processing at Fairchild Semiconductor Corporation was what really threw the floodgates open to extremely reliable silicon transistors and microchips of endlessly growing complexity.

The junction transistor's inventor, William Shockley, dimly perceived this bright future, but he lacked the management skills to bring it off under his direction. In the early 1960s, he began teaching at Stanford University, first as a lecturer and then as a professor of engineering and applied science, while his company slowly failed and was eventually dissolved. Yet without Shockley's contributions in bringing together this stellar group of researchers and introducing them to silicon technology, there would be no Silicon Valley-at least not in Northern California.

## **About the Author**

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- 10. Soon after Bell Labs research director Mervin Kelly hired Shockley in 1936, he impressed on his new employee the needs of the Bell System to replace its unreliable electromechanical switches with a better, faster solid-state version. Kelly's urgings helped stimulate Shockley to invent the junction transistor and probably promoted his interest in the four-layer diode. See Riordan and Hoddeson, *Crystal Fire*, pp. 81-82, W. W. Norton & Co., New York (1997).
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Exposed *p-n* Junctions at the Surface of Silicon Transistors by Oxide Masking Techniques," 14 January 1959, copy provided courtesy of Jay Last.

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- Robert N. Noyce, U.S. Patent No. 2,981,877, "Semiconductor Device-and-Lead Structure," filed 30 July 29. 1959, awarded 25 April 1961. Here it is crucial to note that lack Kilby had conceived similar ideas several months earlier at Texas Instruments, and that the two men are generally perceived as the co-inventors of the integrated circuit. Kilby, however, did not have any idea of the planar technology used in the Noyce patent, and proposed that individual components on a chip be connected by what became known as "flying wires." See Jack Kilby, IEEE Transactions on Electron Devices, 23, 648 (July 1976); and Michael S. Wolff, "The Genesis of the Integrated Circuit," IEEE Spectrum (August 1976), pp. 38-45.
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