A Scientist's Perspective on the Early Days of MOS Technology

by Bruce E. Deal

In September 1957, Frosch and Derick of Bell Telephone Laboratories published a seminal paper in the *Journal of The Electrochemical Society* concerning the use of silicon dioxide as a selective mask against dopant diffusion into silicon wafers. This oxide layer was soon shown to passivate the underlying p-n junctions. Subsequent Bell Labs work involved the fabrication of both bipolar and the newly developed metal-oxide-semiconductor, or MOS, transistors. At about the same time, Jean Hoerni of Fairchild Semiconductor Corporation in Palo Alto, California, developed the so-called planar process, in which the diffused junctions were left covered by the masking oxide during subsequent device fabrication and operation. This process quickly began to revolutionize the semiconductor industry.

Not too long after that, in the early 1960s, several industrial laboratories—RCA, Sprague Electric, Westinghouse, Texas Instruments, General Electric, IBM, and others—initiated research programs involving investigation of thermally oxidized silicon structures. These programs were aimed at eventually developing MOS devices, which made use of these metal-oxide-silicon sandwiches and their associated structures. Fairchild Semiconductor was no exception, in 1963 assembling a research team that began a series of MOS projects.

The following section summarizes the Fairchild oxide program during the years 1963-1979. Related investigations continued there well into the 1980s. Numerous papers were presented and/or published by the various Fairchild investigators involved in subjects related to thermal oxidation during the entire time. Even by 1970, more than 25 technical papers on the oxidation of silicon had been published.

Fairchild Oxidation Investigations (1963-1979)

Starting in 1963, the primary members of the Fairchild oxidation group were Gordon Moore and C. T. Sah. Bruce Deal, Andy Grove, and Ed Snow joined Fairchild R&D in early 1963, with Frank Wanlass already on board. Several other support personnel joined the activity late in 1963. The overall goal at Fairchild was to obtain a better understanding of the thermally oxidized silicon system with emphasis on developing stable and reproducible MOS devices. Currently available bipolar devices were expected to be improved as well. It was soon obvious that considerable competition developed among the various oxide groups established by other electronic companies, as noted above.

Members of the Fairchild oxide team had various backgrounds (physical chemistry, chemical engineering, physics, electrical engineering). These diverse backgrounds provided a good basis for the challenges soon encountered. Assistance was provided by consultants previously at Bell Labs and Stanford University. Technical information was obtained from attendance at technical meetings and from technical papers. Several Fairchild investigators had worked at Rheem Semiconductor (first spin-off of Fairchild), and Bruce Deal had published preliminary results obtained there in 1962 involving silicon oxidation kinetics. Some of those results were reported at the 1962 ECS fall meeting in Los Angeles by Deal and Fairchild personnel. Many personnel in the field also presented their experimental findings at the newly formed Silicon Interface Specialists Conference (SISC) meetings sponsored by the IEEE beginning in 1962.

A list of highlighted Fairchild publications (mainly by Deal, Grove, Snow, and Sah) published from 1965 to 1981, which dealt with the oxidized silicon system, is presented in Table I. Five of these publications are discussed in more detail in subsequent sections. The subjects of these projects serve to identify the thrust of this early Fairchild silicon thermal oxide research.

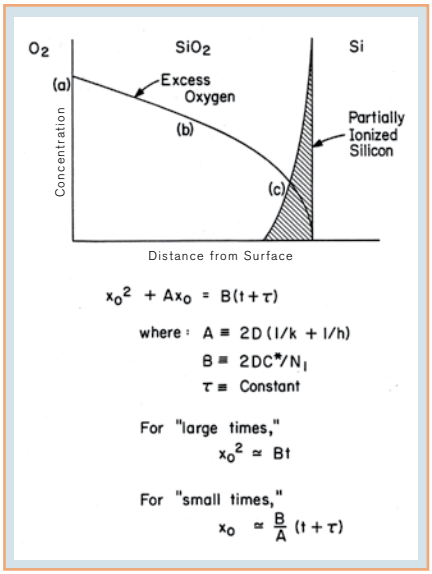

Fig. 1. *Kinetics of silicon thermal oxidation.*

Projects – General Detail

Silicon Thermal Oxidation Kinetics.—Following the preliminary studies of silicon thermal oxidation kinetics by Deal and coworkers at Rheem Semiconductor in Mountain View, CA, and reported at the fall, 1962 ECS meeting, a more complete investigation was initiated in 1963 at Fairchild R&D by Deal and Grove. The so-called "Deal-Grove" oxidation model, *Thermal Oxidation Kinetics Model*, published in 1965 in the *Journal of Applied Physics* (see Table I, Ref. 1), was one of the most cited in semiconductor technology and was the basis for numerous future publications by Fairchild and other organizations. Typically, silicon thermal oxidation is accomplished by reacting silicon in oxygen (O_2) and/or water vapor (H_2O) at 800-1250° C. Based on a combination linear-parabolic model, the relationship is summarized by an

Table I. Thermally Oxidized Silicon References: Highlights of Fairchild R&D (1965-1981).

1. Thermal Oxidation Kinetics Model, Deal, et al., *J. Appl. Phys.*, **36**, 3770 (1965).
2. MOS C-V Model, Grove et al., *Solid State Elect.*, **8**, 145 (1965).
3. Ion Transport in Thermal Oxides, Snow, et al., *J. Appl. Phys.*, **36**, 1664 (1965).
4. Thermal Oxidation of Si in Various Ambients, Hess, at al., *J. Electrochem. Soc.*, **122**, 529 (1975).
5. Charges in Thermally Oxidized Si, Deal, et al., *J. Electrochem. Soc.*, **121**, 198C (1974).
6. Barrier Energies in Oxidized Si, Deal, et al., *J. Phys. Chem. Solids*, **27**, 1873 (1966).
7. Polar Effects in Oxidized Films, Snow, et al., TMS-AIME, **242**, 512 (1968).
8. Heavily-Doped Si Effects on Oxidation, Deal, et al., *J. Electrochem. Soc.*, **112**, 430 (1965).
9. Charge Terminology, Deal, at al., J. Electrochem. Soc., **127**, 979 (1980); *Semiconductor Silicon/1977*, H. R. Huff and E. Sirtl, Editors, PV 77-2, p. 276, The Electrochemical Society proceedings Series, Pennington, NJ (1977); *IEEE Trans. Electron Devices*, **ED-27**, 606 (1980).
10. Kinetics of High Pressure Silicon Oxidation, Razouk, et al., *J. Electrochem. Soc.*, **128**, 2214 (1981).

equation of the form $x_o^2 + Ax_o = B(t + \tau)$, indicated in Fig. 1, where x_o = oxide thickness, t = oxidation time, and A, B, and τ are constants. The shift in the time coordinate, τ, is an empirical correction factor related to the thickness of the initial oxide layer, x_i. Thermal oxidation proceeds by three consecutive reactions: (a) silicon oxide surface oxidant adsorption, (b) oxygen diffusion through the oxide, and (c) Si-SiO_2 interface reaction. The parabolic constant B includes the effective oxidant diffusion coefficient (D_{eff}), which includes the effect of space charge on the rate of transport, C^* is the equilibrium concentration of oxidant in the oxide and is proportional to the partial pressure of the oxidant in the gas by Henry's Law, and N_1 is the number of oxidant molecules incorporated into a unit volume of the oxide layer. B/A is a function of the surface reactions and is referred to as the linear rate constant, under appropriate conditions. Several of these factors are involved in subsequent investigations discussed below. It should be noted that MOS layers of oxide thickness of 20 to 200 nm could be reproducibly prepared using the equation in Fig. 1. The model was used in various modeling programs, including Stanford SUPREM. Below 20 nm, a different mechanism takes over, which is still not understood completely. Generally, empirical data must be used in this range.

MOS Capacitance–Voltage (C–V) Model for Investigating Thermally Oxidized Silicon Structures.—With the development of the planar passivation process at Fairchild and the MOS transistor at Bell Labs in 1959-1960, investigators began to look for a simple method for characterizing the thermally oxidized silicon structure. Earlier techniques employed more complicated field-effect structures where the change in conductance of an MOS device was determined as a function of gate bias. It was soon found that the capacitance-voltage (C–V) relationship was simpler to obtain and monitor (See Table I, Ref. 2). Such was the case at Fairchild. Without going into detail, the nature of the Si-SiO_2 interface could be characterized by the C–V method of analysis. Examples of C–V plots are shown in Fig. 2 (left-hand side), with their corresponding charge models on the right-hand side (see the section below on "Charges in Thermally Oxidized Silicon"). The experimental curves can be compared with theory, and properties such as fixed and mobile oxide charges, oxide thickness, average doping density in the surface space charge region, work function differences and other properties can be determined by observing the voltage dependence or shape of the C–V plot. The dependence of interface characteristics as a function of surface doping concentration, oxide thickness and measurement frequency can also be measured. Much of Fairchild's subsequent oxide research (as well as that of other organizations) made use of the MOS C–V procedure for Si-SiO_2 characterization. The parameters used in Fig. 2 represent terminology used in the early days of MOS C–V characterization. The term "Q_{ss}" originally intended to describe what we now call "Q_f", became so widely used for various effects that the new definitions to be described below became a necessity.

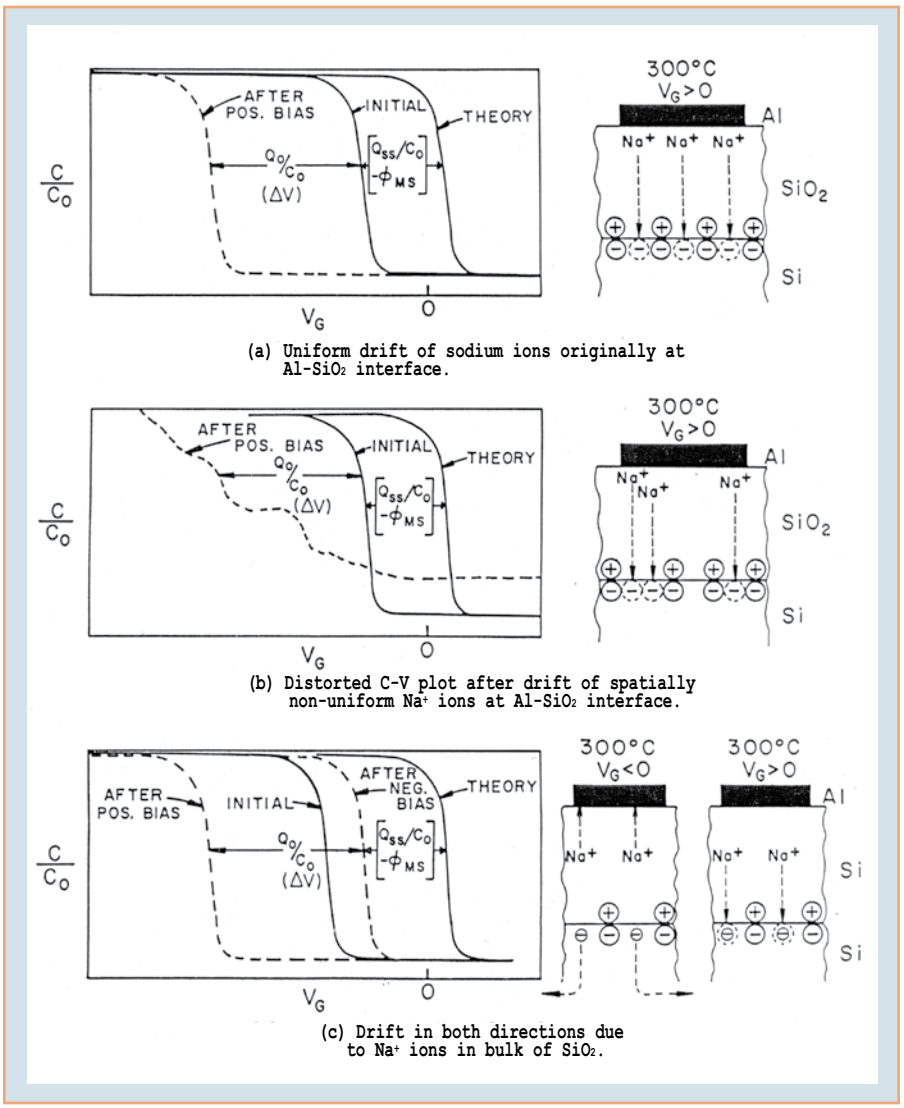

Fig. 2. *C-V plots of three types of ion drift.*

Table II. Fairchild Investigators Who Studied Ambient Effects on Thermal Oxidation.

P. Castro	H_2 (N_{it})	1971
D. Hess	O_2/N_2 (Kinetics)	1975
D. Hess	O_2/N_2 (Oxide charges)	1975
D. Hess	O_2/HCl	1977
B. Deal	O_2/Cl_2	1978
B. Deal	Pyro/H_2O	1978
B. Deal	O_2/HCl; H_2O/HCl	1978
R. Razouk	High Pressure H_2O	1981
J. Rouse	O_2/HCl	1981
R. Razouk	H_2	1982
L. Lie	High Pressure O_2	1982
J. Rouse	O_2/HCl	1984
J. de Larios	Surface Clean	1987

Ion Transport in Thermal Oxides.—As oxidized silicon structures suitable for fabricating potential MOS devices were characterized, it was soon found (at Fairchild and competitors) that they were very unstable electrically. Using C–V analysis, voltage biased, 200 nm thick oxide gate flat-band voltages (V_{fb}) were found to "drift" 50 volts or more at temperatures of 200°C or lower. These results led to on-going speculation at technical meetings as to the source of these instabilities. Some of the proposed sources were surface ion migration, hetero-junctions, oxygen vacancies, slow oxide traps, protons, polar molecules, and other effects. It turned out that one of the Fairchild team members (Ed Snow)

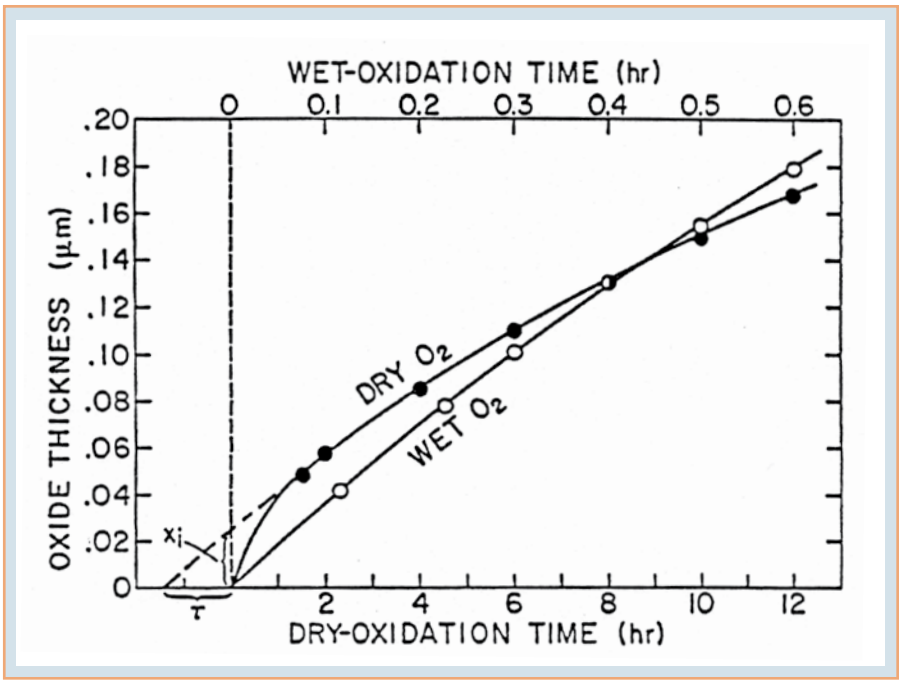

Fig. 3. *H_2O and dry O_2 silicon oxidation kinetics.*

had just completed his PhD research, which was concerned with impurity ion migration through thin oxide layers. Subsequent analysis demonstrated that the main instability was due to alkali ions (Na^+, Li^+, etc.) which were common processing impurities (see Table I, Ref. 3). Various techniques were developed to address this problem, such as electron beam aluminum gate deposition, choice of aluminum gate material, improved cleaning, phosphorus gettering, proper analysis, and so on. These improvements resulted in stable and reproducible MOS device characteristics, which have continued to be effective until the present time. It has also been found that similar material and process control has resulted in improved bipolar devices as well. C–V analysis has continued to be a key monitoring method for the semiconductor industry in general (see Fig. 2).

Ambient Effects on Thermal Oxidation Kinetics.—As described above, silicon thermal oxidation kinetics were first investigated in the early 1960s. During subsequent years, modifications of the dry O_2 oxidation ambient were found to provide certain device advantages (see Table I, Ref. 4). These modifications (see Fig. 3) included dry O_2/H_2O (increased formation rate in H_2O as can be seen by comparing the time scales for H_2O and dry O_2). Additional ambients included: O_2/N_2 (dilution of O_2 with N_2 is done to permit higher oxidation temperatures to enhance dopant diffusion in conjunction with a smaller growth of oxide); O_2/HC1 (alkali contaminate gettering); O_2/pyrogenic (flame) H_2O, high-pressure O_2 or H_2O (increased oxidation rate/decreased process temperature); and H_2 anneal at low temperatures (interface trap anneal). These published papers primarily reported oxidation data in addition to passivation results. Certain observations were noted, such as the fact that while the O_2 diffusion in silicon oxide is greater than for H_2O, the latter has a solubility three times greater than for O_2. This results in a much higher oxidation rate for H_2O as seen in Fig. 3. Table II provides a list of Fairchild investigators who studied and reported combination effects of various ambients. Certainly, this list may be significantly expanded considering the research of others in the field.

Charges in Thermally Oxidized Silicon.—The mobile ionic charges (Na^+, Li^+) were shown to cause instabilities in the as-prepared test structures, as well as MOS device operation in the early 1960s. These mobile ionic charges were found to be only one of four types of charges present in thermally oxidized silicon films (see Fig. 4). Two of these were fixed oxide charge (Q_f) and interface trapped charge (Q_{it}). They were both more stable than mobile ions (Q_m), but also adversely affected MOS device characteristics. They also both appeared to be associated with the final temperature treatment, and were either in the oxide near the Si–SiO_2 interface (Q_f), or directly at the interface (Q_{it}). These are depicted in Fig. 5, along with the proposed diffusion and interface reaction of the oxidant in an MOS structure. Their density could be varied by the final oxidation and/or annealing temperature conditions. A direct correlation between Q_f and Q_{it} was observed, and both were proposed to be due to missing Si-O bonds in the interface region. A number of these and related investigations were conducted and reported by Fairchild researchers over several years in the 1960s and 1970s (see Table I, Ref. 5).

One other charge type, oxide trapped charge (Q_{ot}), was identified in thermally oxidized silicon. These were also due to broken Si-O bonds, but could be located throughout the oxide. They were often caused by ionizing radiation effects, and could be annealed out or otherwise minimized at temperatures as low 200-300°C.

One other effect to be mentioned regarding silicon oxide charge in general was that while Q_f and Q_{it} were formed

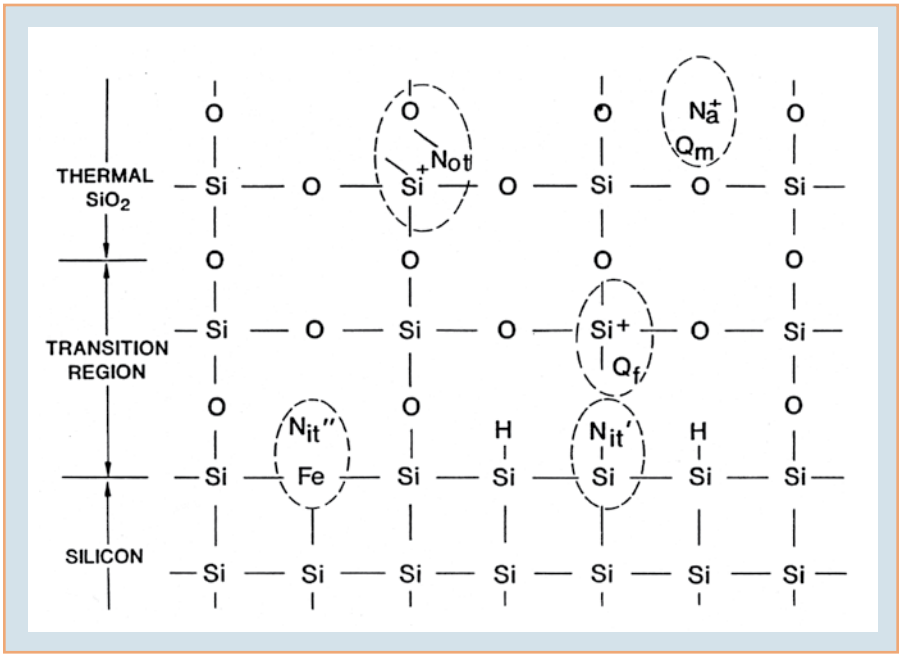

Fig. 4. *Charges in thermally oxidized silicon.*

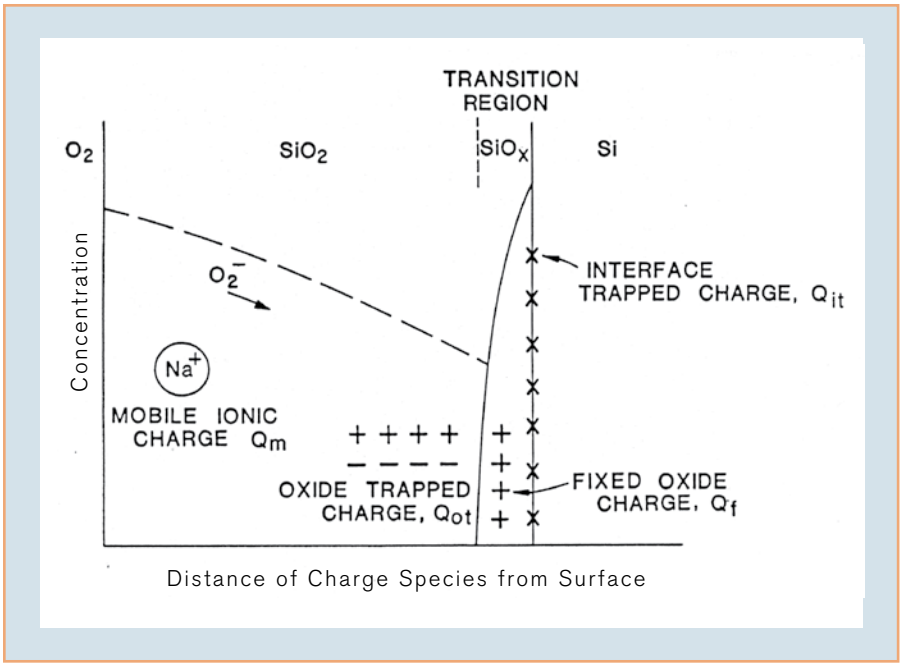

Fig. 5. *Distribution of charges in thermally oxidized silicon.*

and annealed by higher temperature processing, interface traps could also be complexed by hydrogen or hydrogen bearing species treatment at temperatures as low as 300°C and were subsequently made ineffective. This latter process has also been referred to as the "Alneal," the low-temperature nitrogen annealing of aluminum-gate MOS structures. In this process, the *nascent hydrogen* thermally released from the aluminum gate/moisture-contaminated SiO_2 interface migrates to the silicon dioxide-silicon interface, resulting in the annealing of N_{it}.

A final note is that when various research groups were investigating charge effects related to MOS structures, considerable confusion arose concerning symbols used to designate their name and nomenclature. This confusion was reasonably well resolved, however, by committees and publications provided by both the ECS Electronics & Photonics Division and the IEEE Electron Device Society (see Table I, Ref. 9).

Summary

The contributions of scientists and engineers at the Fairchild Research Laboratory regarding thermally oxidized silicon properties in the 1963-1979 time period have been summarized. The results of these investigations helped to advance the understanding, and thus the successful fabrication of stable metal-oxide-semiconductor (MOS) devices and their implementation into the industry. Fairchild's efforts included numerous publications and presentations in oxidation kinetics, oxide charge understanding and control, device yield and stability, and other improved electrical and physical properties of virtually all types of device structures.

A summary of the silicon dioxide technologies discussed herein, "*Thermal Silicon Dioxide—A Unique Dielectric in Semiconductor Technology*," was also presented at the ECS Symposium on "Progress and Opportunities in Dielectric Science and Technology Over the Last 25 Years: A Retrospective," in celebration of the ECS Centennial Meeting (spring 2002). It has been noted by many personnel that the replacement of silicon dioxide by a high-k dielectric, a major currently proposed (and implemented in some cases) change in MOSFET device and process technology, has a significant progeny to emulate. ■

About the Author

Bruce E. Deal died on April 17, 2007, in Palo Alto, California. (See the summer 2007 issue of *Interface* for the complete obituary notice.) Dr. Deal received an AB degree from Nebraska Wesleyan University in 1950, and MS and PhD degrees in physical chemistry from Iowa State University in Ames, Iowa in 1953 and 1955 respectively. In 1959, Deal moved to Palo Alto, CA and spent the rest of his career in Silicon Valley. He first conducted semiconductor research at Rheem Semiconductor in Mountain View, the first spin-off of Fairchild Semiconductor. In 1963, he joined Fairchild's R&D Laboratory in Palo Alto, initially as a Member of Technical Staff and later as a Research Manager/Department Director. After Moore and Noyce founded Intel in 1968, Deal remained at Fairchild until the company was sold to National Semiconductor in 1977. He spent a year at National as Principal Technologist, and then joined Advantage Production Technology as Vice-President of Development. Advantage developed vapor phase wafer cleaning equipment. Deal retired when the company closed in 1992. Deal was a consulting professor at Stanford and Santa Clara Universities for more than twenty five years. Dr. Deal was the recipient of several of the most prestigious ECS awards: ECS Fellow (1991), the ECS Gordon E. Moore Medal for Outstanding Achievement in Solid State Science and Technology (1993), and the ECS Edward Goodrich Acheson Award (2002).

A Note from the Guest Editors

We expected that Bruce's article for this issue of *Interface* would be his last. It was quite clear that this was a somewhat difficult task for Bruce; not the thoughts, per se, which indeed Bruce had introduced to the integrated circuit (IC) community over the past 45 years, but the physical effort at writing them. Ever the scientist, Bruce sent to one of us (HRH) a typed copy of the manuscript, which I dutifully critiqued. I advised his wife, Rachel Deal, of this plan to submit the "reviewed" version back for Bruce's assessment, whereupon Bruce, ever the clever wit, told Rachel to "write deceased on the manuscript" and let me handle it. With the introduction of the Frosch/Derrick paper fifty years ago, perhaps it is fitting, though certainly an ironic if not cruel trick, that the endpoint be placed on this heroic "silicon oxide technology era" with the passing of Bruce Deal as this issue was being prepared. The editors wish to acknowledge the fine assistance of George Brown in the conversion of original draft manuscript into its present form.