A Scientist’s Perspective on the Early Days of MOS Technology

by Bruce E. Deal

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Some of the proposed semiconductor structures related to thermal oxidation during the early days of MOS were later developed into the MOS capacitance model. Consequently, the term “Q” was introduced to describe what we now call “Q of the oxide.” The parameters used in the MOS capacitance model are used to characterize the thermally oxidized silicon structure. The term “Q” was originally intended to describe what we now call “Q.”

More transparent to the reader than the C-V curve is the construction of the C-V curves. C-V analysis, voltage biased, 200 nm (at Fairchild and competitors) that they were found to “drift” by 50 volts or more. This instability was found to be improved as well. It was soon obvious that considerable work was involved in developing this model. The term “Q” was introduced to describe what we now call “Q.”

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Not too long after that, in the early 1960s, several industrial laboratories—BCE, Sprague Electric, Westinghouse, Texas Instruments, General Electric, IBM, and others—began programs involving investigation of thermally oxidized silicon structures. These projects were aimed at eventually developing MOS devices, which made use of the metal-oxide-silicon sandwiches and their associated structures. Fairchild Semiconductor was no exception. In 1963, assembling a research team that began a series of technical meetings and from technical papers.

The following section summarizes the Fairchild oxidation program during the years 1963-1979. Related investigations continued there well into the 1980s. Numerous papers were presented or published by the various Fairchild investigations involved in subjects related to thermal oxidation during the entire time. Even by 1970, more than 25 technical papers on the oxidation of silicon had been published.

Fairchild Oxidation Investigations (1963-1979)

Starting in 1963, the primary members of the Fairchild oxidation group were Gordon Moore, John Rouse, Bruce Deal, Andy Grove, and Ed Snow joined Fairchild R&D in early 1963, with Henry Huff and Ed Snow, who had joined Fairchild earlier in the year. The group was led by Bruce Deal, and the Fairchild oxide team had various backgrounds (physical and applied sciences, electrical engineering, chemical engineering, etc.). The Fairchild oxidation group was expected to obtain a better understanding of the thermally oxidized silicon system, which made use of these metal-oxide-semiconductor structures. The so-called "Deal-Grove" oxidation model, Thermal Oxidation Kinetics Model, published in 1965 in the Journal of Applied Physics, was one of the most cited in semiconductor technology and was the basis for numerous future publications by Fairchild and other oxidation research groups. The thermal oxidation was accomplished by reacting silicon in oxygen ($O_2$) and/or water vapor ($H_2O$) at 800-1200°C. Based on a combination linear-parabolic model, the relationship is summarized by an equation of the form $x^2 + A_x = B(t + 1)$, indicated in Fig. 1, where $x$ - oxide thickness, $t$ - oxidation time, and $A$, $B$, and $r$ are constants. The shift in the time coordinate, $t$, is an empirical correction factor related to the thickness of the initial oxide layer, $x$, thermal oxides and the initial hydroxide film, $H_2O$, which includes the effects of surface recombination on the rate of transport, $C$ is the equilibrium concentration of oxidant in the oxide and is proportional to the partial pressure of the oxidant in the gas by Henry's Law, and $N_2$ is the number of oxidant molecules incorporated into a unit volume of the oxide layer. $B/A$ is a function of the surface reactions and is referred to as the linear rate constant, under appropriate conditions. Several of these factors are involved in subsequent investigations discussed below. It should be noted that MOS layers of oxide thicknesses of 10000 Å or more could be reproducibly prepared using the oxidation in Eq. 1. This model was used in various modeling programs, including Stanford SUPREM. Below 20 nm, a different mechanism takes over, which is still not understood completely. Generally empirical data must be used in this range.

MOS Capacitance-Voltage (C-V) Model for Investigating Thermally Oxidized Silicon Structures—The development of the planar passivation process at Fairchild and the MOS transistor at Bell Labs in 1959-1960, investigators began to look for a simple method for characterizing the thermally oxidized silicon structure. Earlier techniques employed more complicated field-effect structures where the change in conductance of an MOS device was determined as a function of gate bias. It was soon found that the capacitance- voltage (C-V) relationship was simple to obtain and monitor (see Table I, Ref. 2). Such was the case at Fairchild. Without going into detail, the nature of the Si-SiO$_2$ interface could be characterized by the C-V model of analysis. Examples of C-V plots are shown in Fig. 2 (left-hand side), with their corresponding charge models on the right-hand side (see the section below on "Charges in Thermally Oxidized Silicon Structures") and $Q_{ox}$, which includes the effect of space charge region, work function differences and other properties can be determined by observing the voltage dependence or shape of the C-V plot. The dependence of interface recombination and space charge region, work function differences and other properties can be determined by observing the voltage dependence or shape of the C-V plot. The dependence of interface recombination and space charge region, work function differences and other properties can be determined by observing the voltage dependence or shape of the C-V plot.

Table I. Fairchild Investigators Who Studied Ambient Effects on Thermal Oxidation.

<table>
<thead>
<tr>
<th>Name</th>
<th>Institution</th>
<th>Years</th>
</tr>
</thead>
<tbody>
<tr>
<td>P. Castro</td>
<td>RCA</td>
<td>1971</td>
</tr>
<tr>
<td>D. Hess</td>
<td>IBM</td>
<td>1973</td>
</tr>
<tr>
<td>H. R. Huff</td>
<td>Bell Labs</td>
<td>1975</td>
</tr>
<tr>
<td>D. Hess</td>
<td>IBM</td>
<td>1976</td>
</tr>
<tr>
<td>B. Deal</td>
<td>RCA</td>
<td>1978</td>
</tr>
<tr>
<td>D. Hess</td>
<td>IBM</td>
<td>1982</td>
</tr>
<tr>
<td>R. Razouk</td>
<td>RCA</td>
<td>1984</td>
</tr>
<tr>
<td>J. de Larios</td>
<td>General Electric</td>
<td>1985</td>
</tr>
<tr>
<td>J. Rouse</td>
<td>IBM</td>
<td>1986</td>
</tr>
</tbody>
</table>

Fig. 2. C-V plots of three types of ion drift.

Fig. 1. Kinetics of silicon thermal oxidation.
Charges in Thermally Oxidized Silicon—The mobile ionic charges (Na⁺, Li⁺) were shown to cause instabilities in the as-prepared test structures, as well as MOS device operation in the early 1960s. These mobile ionic charges were found to be the only one of four types of charges (Na⁺, Li⁺, O⁻, or H⁻) in thermally oxidized silicon films (Fig. 4). Two of these were fixed oxide charge (Qₓ) and interface trapped charge (Qₓ). They were both more stable than mobile ions (Qₓ), but also adversely affected MOS device characteristics. They also both appeared to be associated with the final temperature treatment, and were either in the oxide near the Si–SiO₂ interface (Qₓ) or directly at the interface (Qₓ)—these are depicted in Fig. 5, along with the proposed ion and interface reaction of the oxidant in an MOS structure. Their density could be varied by the final oxidation and/or annealing temperature conditions. A direct correlation between the density of Qₓ, or Qₓ, was observed, and both were proposed to be due to missing Si–O bonds in the interface region. A number of these and related investigations were conducted and reported by Fairchild researchers over several years in the 1960s and 1970s (see Table I, Ref. 5).

One other charge type, oxide trapped charge (Qₓ), was identified in thermally oxidized silicon. These were also due to oxide trapping, greater than for H₂O, the latter has a solubility three times greater than for O₂. This results in a much higher oxidation rate for H₂O as seen in Fig. 3. Table II provides a list of Fairchild investigators who studied and reported the combination effects of various ambients.

Certainly, this list may be significantly expanded considering the research of others in the field.

anneal at low temperatures (interface anneal). These published papers primarily reported oxidation data in addition to passivation results. Certain observations were noted, such as the fact that while the O₂ diffusion in silicon oxide is greater than for H₂O, the latter has a solubility three times greater than for O₂. Results in a much higher oxidation rate for H₂O as seen in Fig. 3. Table II provides a list of Fairchild investigators who studied and reported the combination effects of various ambients.

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and annealed by higher temperature processing, interface traps could also be complexed by hydrogen or hydrogen bearing species treatment at temperatures as low as 300°C and were subsequently made ineffective. This latter process has also been referred to as the "Alain," the low-temperature native oxide annealing of aluminum-gate MOS structures. In this process, the nascent hydrogen thermally released from the aluminum gate/moisture-contaminated SiO₂ interface migrates to the silicon dioxide/Interface resulting in the annealing of Nₓ. A real note is that when various research groups were investigating charge effects related to MOS structures, considerable confusion arose concerning symbols used to designate their name and nomenclature. This confusion was reasonably well resolved, however, by committees and publications provided by both the ECS Electronics & Photonics Division and the IEEE Electron Device Society (see Table I, Ref. 9).

Summary

The contributions of scientists and engineers at the Fairchild Research Laboratory regarding thermally oxidized silicon properties in the 1963-1979 time period have been summarized. The results of these investigations helped to advance the design and development of MOS devices and their implementation into the industry. Fairchild's efforts included numerous publications and presentations in oxidation kinetics, oxide charge considerations, control, device design yield and stability, and other improved electrical and physical properties of virtually all types of device structures.

A summary of the silicon dioxide technologies discussed herein, "Thermal Silicon Dioxide—A Unique Dielectric in Semiconductor Technology," was also presented at the ECS Symposium on Progress and Opportunities in Dielectric Science and Technology Over the Last 25 Years: A Retrospective," the celebration of the ECS Centennial Meeting (spring 2002). It has been noted by many persons that the replacement of silicon dioxide by a high-k dielectric, a major currently proposed (and implementing, in some cases) change in MOSFET device and process technology, has a significant propensity to emulate.

About the Author

Bruce E. Deal died on April 17, 2007, in Palo Alto, California. (See the summer 2007 issue of Interface for the complete obituary.) Dr. Deal received an AB degree from Nebraska Wesleyan University in 1950, and MS and PhD degrees in physical chemistry from Iowa State University in Ames, Iowa in 1953 and 1955 respectively. In 1959, Deal moved to Palo Alto, CA and spent the rest of his career in Silicon Valley. He first conducted semiconductor research at Rheem Semiconductor in Mountain View, the first spin-off of Fairchild Semiconductor. In 1963, he joined Fairchild's R&D laboratory and was part of the team that launched the first integrated circuit (IC) community over the past 45 years, but the physical effort at writing this book, even for a scientist, Bruce, sent me to one of us (HRH) a typed copy of the manuscript, which I dutifully critiqued. I advised his wife, Rachel Deal, of this wish to acknowledge the fine assistance of the ECS and the IEEE Electron Device Society for the complete present form. The editors and the ECS Edward Goodrich Acheson Award (2002).

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A Note from the Guest Editors

We expected that Bruce’s article for this issue of Interface would be his last. It was quite clear that this was a somewhat difficult task for Bruce, not the thoughts, per se, which indeed Bruce had introduced to the integrated circuit (IC) community over the past 45 years, but the physical effort at writing this book, even for a scientist, Bruce, sent me to one of us (HRH) a typed copy of the manuscript, which I dutifully critiqued. I advised his wife, Rachel Deal, of this wish to acknowledge the fine assistance of the ECS and the IEEE Electron Device Society for the complete present form.

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had just completed his PhD research, which was concerned with minority ion migration through thin oxide layers. Subsequent analysis demonstrated that the main instability was due to alkali ions (Na, Li, etc.) which were common and occurring impurities in the starting materials. Various techniques were developed to address this problem, such as electron beam induced aluminum gate deposition, choice of aluminum gate material, improved cleaning, photomicroscopy, gettering process and so on. These improvements resulted in stable and reproducible MOS device characteristics, which have continued to be effective until the present time. It has also been found that similar material and process control has resulted in improved bipolar devices as well. C-V analysis has continued to be a key monitoring method for the semiconductor industry in general (see Fig. 2).

**Ambient Effects on Thermal Oxidation**

As described above, silicon thermal oxidation kinetics were first investigated in the early 1960s. During subsequent years, modifications of the dry O2 oxidation ambient were found to provide certain device advantages (see Table I, Ref. 5). Additional ambient effects included O3/N2 dilution of O2 with N2 is done to enhance dopant diffusing, N2O3 pyrogenic (flame) H2O, high-pressure H2 and H2O (increased oxidation rate/decreased process temperatures); and H2 anneal at low temperatures (interface layer). These published papers primarily reported oxidation data in addition to passivation results. Certain observations were noted, such as the fact that while the O2 diffusion in silicon oxide is smaller for H2O, the latter has a solubility three times greater than for O2. This result in a much higher oxidation rate for H2O as seen in Fig. 3. Table II provides a list of Fairchild investigators who studied and reported the combination effects of various ambients. Certainly, this list may be significantly larger, as they were first investigated in the early 1960s. These mobile ionic charges (Qo, Qb) were shown to cause instabilities in MOS device operation in the early 1960s. These mobile ionic charges were found to be one of four types of charges that can develop in thermally oxidized silicon films (see Fig. 4). Two of these were fixed oxide charge (Qf) and interface trapped charge (Qt). They were both more stable than mobile ions (Qo, Qb), but also adversely affected MOS device characteristics. They also both appeared to be associated with the final temperature treatment, and were either in the oxide near the Si–SiO2 interface (Qi), or directly at the interface (Qo). These are depicted in Fig. 5, along with the combination of the previous and interface reaction of the oxidant in an MOS structure. Their density could be varied by the final oxidation and/or annealing temperature conditions. A direct correlation between Qf and Qb was observed, and both were proposed to be due to missing Si–O bonds in the interface region. A number of these and related investigations were conducted and reported by Fairchild researchers over several years in the 1960s and 1970s (see Table I, Ref. 5).

One other charge type, oxide trapped charge (Qt), was identified in thermally oxidized silicon. These were also due to oxygen deficient oxide which was trapped throughout the oxide. They were often caused by ionizing radiation effects, and could be annealed out or otherwise minimized at temperatures as low as 200–300°C.

One other effect to be mentioned regarding silicon oxide charge in general was that while Qo and Qb were formed and annealed by higher temperature processing, interface traps could also be complexed by hydrogen or hydrogen bearing species treatment at temperatures as low as 300°C and were subsequently made ineffective. This latter process has also been referred to as the "Alnecal," a low-temperature nitridation-annealing of aluminum-gate MOS structures. In this process, the nascent hydrogen thermally released from the aluminum gate/moisture-contaminated SiO2 interface migrates to the silicon dioxide/silicon interface resulting in the annealing of Nv.

A final note is that when various research groups were investigating charge effects related to MOS structures considerable confusion arose concerning symbols used to designate their name and nomenclature. This confusion was reasonably well resolved, however, by committees and publications provided by both the ECS Electronics & Photonics Division and the IEEE Electron Device Society (see Table I, Ref. 9).

**Summary**

The contributions of scientists and engineers at the Fairchild Research Laboratory regarding thermally oxidized silicon properties in the 1963–1979 time period have been summarized. The results of these investigations helped to advance the understanding, and thus the successful fabrication of stable metal–oxide–semiconductor (MOS) devices and their implementation into the industry. Fairchild's efforts included numerous publications and presentations in oxidation kinetics, oxide charge understanding, device control, device yield and stability, and other improved electrical and physical properties of virtually all types of device structures.

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