Silicon Surface and Interface Issues for Nanoelectronics

by Yves J. Chabal and Leonard C. Feldman

To a large extent, the silicon revolution is based on the wonderful properties of the silicon/silicon dioxide interface. The importance of this structure has been documented and cited in many articles and books on the history of technology.[1-3] Clearly, it is the most important materials interface in current process technologies.

Briefly, oxidation of silicon results in a large bandgap, uniform, dielectric layer of amorphous SiO_2, with the proper band-offsets to allow both p- and n-channel devices to be fabricated. Most important, modern growth and annealing techniques result in interface defect levels that are sufficiently small so that carrier transport is close to theoretical limits expected for SiO_2. These excellent qualities have served the community well and been preserved as the basic metal-oxide-semiconductor field-effect transistor (MOSFET) device has scaled down over the last four decades.

Research in the last twenty years has exploited almost every conceivable surface/thin-film probe to establish the underlying physical nature of this critical solid-state interface. Of particular interest has been the nature of the starting silicon surface, the kinetics of the oxidation process, the structure and solid-state chemistry of the silicon-silicon dioxide interface and the relationship of the structure to the electronic properties.

Until recently, our understanding of the growth processes was captured in the Deal-Grove model of oxidation, based on oxygen diffusion and interface reactions.[4] Many studies have shown that this model in not a good representation of growth at the modern scale of ~2 nm, and an atomic level description is required.

Interface structure may be characterized as follows: a very thin suboxide layer (< 2 monolayers) exists, as demonstrated from X-ray photoelectron spectroscopy (XPS) and infrared spectroscopy;[5] a small region (~3 monolayers) of distorted silicon exists within the substrate, below the two monolayer suboxide, as demonstrated by ion scattering;[6] the "as-grown" interface has ~10^{12}/cm^2 dangling bonds with electronic states within the oxide energy gap; and this interface (defect) state density can be reduced to ~10^{10}/cm^2 when the structure is annealed in hydrogen (or forming gas, 95% nitrogen and 5% hydrogen) as indicated by electron paramagnetic resonance and electrical measurements.[7] Transmission electron microscopy verifies the sharp interface and the basic structure described above.

The aspect of nanoscale that has received the most recent attention is the need for an alternate dielectric of higher dielectric constant. In short, scaling demands < 2 nm oxides, which then display quantum mechanical tunneling, revealed as a power consuming leakage current. The solution is a material of higher dielectric constant with greater thickness, to keep the equivalent oxide thickness (EOT) constant, while drastically reducing the tunneling leakage. All desirable features of traditional SiO_2 described above must be preserved. However, new challenges arise as we face the future of nanoscale devices with these different gate dielectric materials. At the nanoscale level, the starting surface plays a critical role in terms of perfection, flatness, and cleanliness. Growth is an evermore delicate process requiring atomic control; and structure, interface perfection, and defect levels must all be confronted again. One prospect that capitalizes on the integrity of silicon oxide, integrates a combined dielectric consisting of interfacial SiO_2 (or SiON) followed by alternate dielectrics. To be viable, this compound dielectric requires an ultrathin, high quality silicon dioxide that once again tests interface science, not only with respect to the silicon substrate but also with respect to the dielectric/dielectric interface. This is the outstanding materials challenge in MOS technology.

In all cases, the community must approach the problem from the atomic level, seeking optimum bonding configurations, monolayer control of growth, and unprecedented control and reliability.[8]

Current Practices and Understanding

Pre-cleaning of silicon surfaces—Aqueous treatment of silicon surfaces is the first step to control the interfaces.[9] Wet etching operates in two ways: it removes oxides and impurities from the surface at relatively low temperatures (<100°C) and terminates the silicon surface either with a hydrogen monolayer or a thin oxide film. In some cases, the process can also modify the structure of the silicon substrate. Given the enormous practical importance of wet chemical treatment of silicon wafers during processing, each aspect of the process has been studied extensively.[9] The removal of (*i*) metal and hydrocarbon impurities is achieved by acid/peroxide solutions (*e.g.*, $HCl/H_2O_2/H_2O$ and $H_2SO_4/O_2/H_2O$), (*ii*) particles by basic solutions that simultaneously oxidize and etch the surface (*e.g.*, $NH_4OH/H_2O_2/H_2O$), and (*iii*) oxides by fluoride solutions that leave the surface H terminated. The mechanisms leading to hydrogen passivation of silicon surfaces by HF etching are now well understood.[10] In particular, the reason that HF etching does not lead to F-termination even though Si-F is more stable than Si-H, is that chemisorption of fluorine on the surface Si atom (upon removal of the last oxygen atom) polarizes the Si-Si back bonds. Thus, while the Si-F bond is stable, the Si-Si back bonds are weakened by this polarization and the complete fluorination of the Si occurs, leaving behind a more neutral (less polar) hydrogen-terminated surface. The initial top silicon surface atom is removed by forming SiF_4 complexes that are dispersed in the solution. Hydrogen passivated surfaces are remarkably stable in the main components of air (oxygen, nitrogen, water vapor)[11] and only become slowly oxidized in air due to radical-mediated reactions. In solutions, hydrogen passivated surfaces may also

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remain stable unless aggressive oxidizing agents are used such as peroxides. The degree and completeness of oxidation varies depending on the exact reagents. Among the four main methods (SC_1, SC_2, piranha, and nitric)[9], the sulfuric/peroxide (piranha or SPM) treatment leads to the most homogeneous, thinnest, and hydrogen-free oxide.[12] Starting with hydrogen-free oxides is important because some aspects of hydrogen within device structures can cause problems (reliability, etc).

An important aspect of wet processing is the potential control of the surface morphology via preferential etching. A beautiful illustration comes from buffered HF etching of Si(111) and Si(100), which makes it possible to slowly etch silicon after the oxide is removed. Such etching is highly preferential, leading to the formation of atomically flat monohydride-terminated Si(111) surfaces[13] and atomically rough, multihydride-terminated Si(100) surfaces (Fig. 1). Similar behavior is observed for etching of H-terminated silicon in hot water[14] and in KOH solutions.[15]

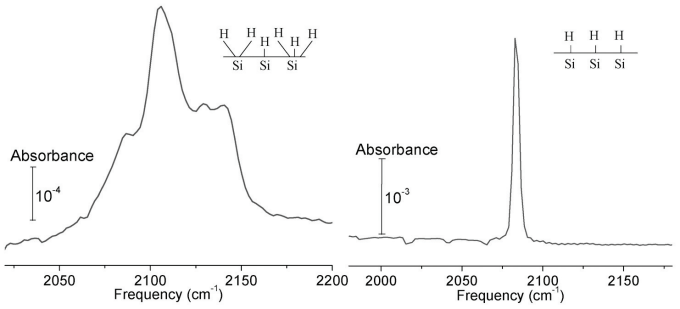

FIG. 1 Infrared absorption spectra of (left) atomically rough H/Si(100) characterized by a broad and structured spectrum representing several hydride termination (mono-, di-, trihydrides) and (right) atomically smooth H/Si(111) surfaces defined by a sharp, resolution limited feature polarized perpendicular to the surface.

Initial oxidation of silicon—Many factors influence silicon oxidation: thermodynamic drive for oxygen agglomeration, kinetic barrier to oxygen surface and bulk diffusion, pathways for oxygen decomposition and strain of silicon oxide in the vicinity of crystalline silicon. It is not surprising that several regimes can be identified, even for the simple oxidation of clean silicon in an ultrahigh vacuum environment.

Regime 1: oxygen insertion into silicon (top silicon double layer): Both O_2 and H_2O oxidation have been studied. The reactants readily dissociate: O_2 into a silanone configuration[16] and H_2O into OH and H, [17] forming metastable structures. Annealing studies clearly show that there is a thermodynamic driving force for oxygen to insert into the back bonds of the surface silicon atoms, and to agglomerate into atomic scale clusters with three oxygen atoms bound to a surface silicon atom. The presence of hydrogen atoms in H_2O dissociation only affects the kinetics of migration.[18] Oxidation of deeper layers (> top double layer) require higher activation energies. Consequently, the first regime of oxidation is characterized by a highly inhomogeneous process, driven by thermodynamics and controlled by kinetic (and chemical) factors.

Oxidation of a hydrogen-passivated silicon surface is emerging as an industrially critical area.[19] Generally, the barriers for oxygen insertion are much higher, particularly for H_2O oxidation,[18,20] and the surface oxide structures are stabilized by hydrogen similar to H_2O oxidation of clean Si. But the nature of the oxidation is similar, with formation of highly oxygen-coordinated structures involving only the top double layer.

For both clean and H-terminated silicon oxidation, the complete layer growth is achieved by two-dimensional oxide island nucleation.[21] As the oxidation nears completion, strain begins to play a role, and to affect the nature of the deeper oxidation.

Regime 2: Layer-by-layer oxidation (beyond the top double layer): After the surface oxide layer becomes continuous (~0.5 nm thick), Hattori has shown using high resolution XPS that the nature of the Si oxidation states vary periodically (period ~ 0.7 nm) as oxidation proceeds.[19] This observation indicates that oxidation occurs at the Si/SiO_2 interface and proceeds layer-by-layer. This behavior extends at least to the first 2 nm of oxide, a depth accessible to XPS. Diffusion of oxygen to the Si/SiO_2 interface with subsequent oxidation has been unambiguously demonstrated by medium energy ion scattering (MEIS) studies[22] using isotopic markers (^{18}O). If a thin oxide involving only ^{16}O (*i.e.*, $Si^{16}O_2$) is further oxidized using only ^{18}O, the isotopic species ^{18}O is found only at the Si/SiO_2 interface (and a small amount at the surface) with no detectable ^{18}O inside the original oxide film, confirming oxygen diffusion through the oxide and reaction only at the lower interface. The presence of a small amount of ^{18}O at the surface may simply reflect isotopic exchange or point to surface reaction as a requirement for subsequent atomic oxygen diffusion. The pressure dependence of the evolution of the ^{18}O peaks in MEIS is distinctly slower than the linear dependence consistent with Deal-Grove behavior.

Future Directions

Silicon oxynitridation—Over a decade ago it was found that adding nitrogen to SiO_2 improves MOSFET properties such as hot electron degradation, dopant diffusion from a heavily doped polygate and results in a somewhat higher dielectric constant (often in the range 5.5-6.5). Deleterious effects of nitrogen additions have also been reported including increased trapped charge and lower inversion layer mobility. For example, while oxynitrides are good diffusion barriers preventing the deleterious diffusion of H, B, and metal diffusion (from high-κ dielectrics), they also limit O_2 and NO penetration, strongly modifying the growth kinetics in a nonlinear manner. Nevertheless the advantages are sufficient for widespread use.

Many oxynitridation/nitridation methods have been employed including thermal growth in N_2, NO, N_2O, NH_3 as well as metallorganic chemical vapor deposition (MOCVD), rapid thermal (RT)CVD, plasma-enhanced (PE)CVD, jet vapor deposition (JVD), and atomic layer (AL)CVD.[23] In addition to these growth techniques shallow N implants into silicon can be incorporated into a grown oxide with some of the same benefits. Both the gas phase and solid-state chemistry of the nitridation process may be complicated. For example, gas-phase N_2O at high temperature rapidly decomposes to its main equilibrium constituents of NO, O_2, and N_2. Because this may occur during the actual exposure, the dynamics of growth may be strongly time dependent. In the solid state there is evidence that oxygen atoms can remove nitrogen through an exchange mechanism, to form the more thermodynamically stable SiO_2. That exchange (and out-diffusion) is more probable near the vacuum surface than the lower interface is part of the explanation for the accumulation of nitrogen at the silicon/dielectric interface, a fortunate circumstance!

High-κ dielectrics growth—The main challenge of amorphous high-κ dielectrics growth is the control of the silicon/oxide interface. Promising materials have been identified (HfO_2, ZrO_2, Al_2O_3) based on their thermodynamic properties. Yet, despite their stability compared to Si and SiO_2, an interfacial SiO_2 layer is formed during growth, even when relatively low-temperature atomic layer deposition (ALD) methods are used. Clearly, the need for *in situ*

characterization during growth is essential. A common starting surface to minimize interfacial SiO_2 formation is the H-passivated silicon surface obtained by HF etching. Dielectric growth directly on such a surface under some circumstances may yield an interfacial SiO_2 layer that is thinner than 1 nm, but it is often not sufficient to ensure 0.5 nm EOT. A value of 0.5 nm is often noted as required for the gate stack system under inversion where MOSFET operation ensues. The solid-state community is now exploring the possibility of further functionalizing the silicon surface, for instance, starting with H-passsivated surfaces as noted above. Additionally, ammonia pretreatments can form a thin nitride layer that effectively prevents SiO_2 formation. Chlorination of H-terminated surfaces has also been demonstrated and proposed as a possible template for high-κ dielectrics growth. The jury is still out on the effectiveness of such pretreatment schemes. In the meantime, deposition of silicates is being explored as a powerful compromise between the larger dielectric constant achievable (often about 15-20) and amorphous oxides/nitrides of lower dielectric constant but more stable interface characteristics.

Another approach is the growth by molecular beam epitaxy (MBE), of crystalline epitaxial oxides directly on clean silicon surfaces. While the growth temperatures are typically higher than for atomic layer deposition (ALD) growth, interface sharpness is better in some cases.

Conclusions

The silicon-based roadmap (International Technology Roadmap for Semiconductors, ITRS), provides a pathway for silicon-based technology until ~2020. Success is heavily dependent on new materials and the gate dielectric layer (and gate electrode) is one of the most critical issues. Whether grown by MOCVD, MBE, ALD, or thermally, ultrathin dielectric films can be achieved only with the highest control of the initial surface chemical configuration and the process itself. This will be accomplished through the tools and techniques of surface science and the creativity of materials scientists. ■

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