# Improved CMOS Performance via Enhanced Carrier Mobility

by P. M. Mooney

The amazing advancements achieved in Si CMOS have come primarily from scaling, *i.e.*, from reducing the critical dimensions of the transistors. Since it is becoming increasingly difficult to further reduce critical dimensions such as the gate oxide thickness, alternative methods of improving transistor performance are being investigated. One approach is to increase the free carrier mobility in the active region of the device. Here we discuss several different ways of accomplishing this.

The mobility of electrons and holes in a semiconductor derives from the band structure of the material. Due to the crystal symmetry of Si, the mobility of electrons and holes varies with the direction of the applied electric field and, therefore, the performance of MOSFETs fabricated in Si depends on the crystal orientation of the substrate. The highest electron mobility is found using Si(100) substrates; however, the highest hole mobility is observed when devices are fabricated in Si(110) substrates. These mobilities are for the <110> direction for both wafer orientations. The drive current for pFETs fabricated on bulk Si(110) substrates was increased by 45% compared to control devices fabricated on Si(100) [1]. In order to obtain the highest mobility for both electrons and holes, hybrid crystal orientation substrates, as shown in Fig. 1, were made using wafer bonding and selective epitaxy methods; nFETS are fabricated on regions of Si(100) and pFETs are fabricated in regions of Si(110)-on-insulator.[1,2] Ring oscillators have been demonstrated with gate delay reduced by 21%.[2] Although there are design and integration challenges, hybrid crystal orientation technology

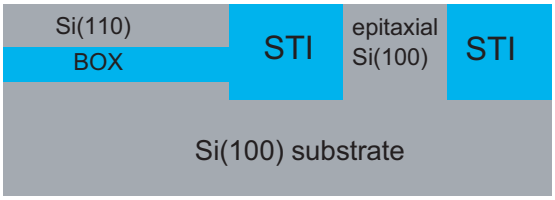


*FIG. 1. Schematic drawing (cross section) of one type of hybrid crystal orientation substrate. The pMOSFET is fabricated in the Si(110) regions and the nMOSFET is fabricated in the epitaxial Si(100) regions. The shallow trench isolation (STI) and the buried oxide (BOX) are $SiO_2$.*

(HOT) is very promising because the fabrication processes are compatible with current VLSI technology and no new materials are introduced.

It has also been demonstrated that carrier mobility is increased when the channel region of the Si MOSFET is under biaxial tensile strain.[3,4] This is typically achieved by means of a strain-relaxed SiGe buffer layer grown on Si(100) substrates, that serves as a "virtual substrate" for the epitaxial growth of a thin strained Si layer.[5,6] Dramatic electron mobility enhancement has been found at low strain, a factor of 1.5-2.0 for strain in the range of 0.4-1.0%.[3,4] Unfortunately, tensile strain of at least 1% is required to overcome hole mobility degradation and hole mobility enhancement factors are lower than for electrons, 1.0-1.4 for tensile strain in the range 1.0-1.9%.[4,7] Strained Si devices fabricated on strain-relaxed SiGe-on-insulator (SGOI) substrates have also been demonstrated.[8] Additionally, similar enhanced electron and hole mobility was recently observed for strained Si devices on ultra-thin strained Si-on-insulator (SSOI) wafers fabricated by transferring the strained Si layer from the virtual substrate using wafer bonding methods.[7]

Although significant carrier mobility enhancements have been demonstrated, there are many challenges for VLSI applications. One challenge is to reduce the density of stacking faults and threading dislocations originating in the strain-relaxed SiGe buffer layer. This is more easily achieved in the case of Ge fraction corresponding to strain of <1% in the Si layer. Another difficulty is that the diffusion of n-type dopants is enhanced as the Ge fraction increases and is, therefore, very difficult to control in very small devices. Although the latter problem is avoided in the case of SSOI, threading dislocations and stacking faults (from the original virtual substrate) are still present in the strained Si layer.

Several methods of producing defect-free strained Si layers have been proposed. One method utilizes a so-called compliant substrate to create islands of Si under tensile strain.[9] Another approach involves the growth of SiGe on free-standing Si slabs supported by a single $SiO_2$ pedestal.[10,11] In this case, strain relaxation is elastic (without the

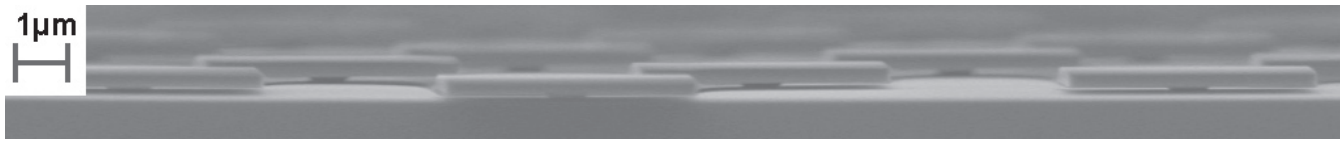


*FIG. 2. (a) SEM image showing an array of free-standing Si/SiGe/Si slabs supported by an $SiO_2$ pedestal on a Si substrate. (b) Raman spectra showing the Si-Si vibrational mode for bulk Si (dashed curve) and for strained Si islands. In order of increasing intensity the three strained Si samples are: as-fabricated after removal of the upper Si and SiGe layers, and heated either to 1070 ˚C or to 1000 ˚C after fabrication[12].*

introduction of misfit dislocations) and the final strain state of the structure is determined by the relative thickness of the SiGe and Si layers. Similarly, metastable structures consisting of a pseudomorphic SiGe layer and a Si cap layer grown on a thin SOI wafer were etched to form free-standing Si/SiGe/Si slabs (see Fig. 2a) that relax elastically when the buried oxide is removed.[12] The Si/SiGe/Si slab was then oxidized and reattached to the substrate using a deposited material, in this case amorphous Si, to fill the space between the slab and the Si substrate.[12] The upper Si and SiGe layers were then removed leaving islands of strained Si-on-insulator (see Fig. 2b). Strained Si layers formed by these methods have a dislocation density that is the same as that in the original pseudomorphic SiGe layer, since no additional dislocations are formed during strain relaxation. Provided the growth of the pseudomorphic SiGe layer is done properly, the dislocation density is many orders of magnitude lower than in bonded SSOI wafers, which have a threading dislocation density of about $5 \times 10^5$ $cm^{-2}$ in the best case.

Another approach to achieve strained Si is by the local application of stress to the Si under the gate of the MOSFET.[13-15] Silicon under uniaxial tensile strain has been achieved by the deposition of stressed silicon nitride films during device processing.[15,16] More recently SiGe grown selectively in the source and drain regions of the MOSFET (see Fig. 3) has been shown to compress the Si under the gate and a hole mobility enhancement of 50% was reported.[16] Advantages of these methods are that both tensile and compressive strain can be implemented locally on the same wafer and that the device fabrication processes are all very similar to those used for standard Si devices. Although the magnitude of the local strain that can be achieved and thus the performance enhancement is limited, local uniaxial strain may be combined with biaxial tensile strain or with HOT to achieve further improvements in device performance than with either method alone. ■

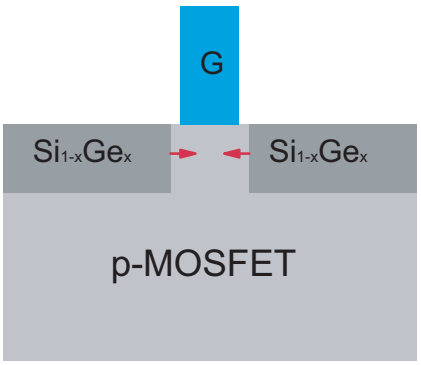


*FIG. 3. Schematic drawing (cross section) of a pMOSFET in which epitaxial $Si_{1-x}Ge_x$ is grown selectively in the source and drain regions. The lattice constant of $Si_{1-x}Ge_x$ is larger than that of Si, and thus the SiGe exerts a compressive force on the Si under the gate (G), as indicated by the red arrows.*

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