Beyond CMOS Electronics: Self-Assembled Nanostructures

by Ted Kamins

When the first transistors were built in the late 1940s, few could predict their widespread adoption and the capabilities of the integrated circuits that would evolve from those initial discoveries. Although the concept of field-effect transistors controlled by an external electrode had been conceived two decades before the first observation of transistor action, the first transistors were bipolar transistors, rather than field-effect transistors, because the interface control needed for practical field-effect transistors was lacking. Extensive efforts throughout the 1960s finally provided the interface control needed for practical use of the presently dominant, insulated-gate field-effect transistors built using the metal-oxide-semiconductor (MOS) system based on silicon and thermally grown silicon dioxide.

Conventional Top-Down Fabrication

Clever processing — especially lithography — allowed ever smaller features on increasingly complex integrated circuits. The small dimensions have been primarily achieved using shorter wavelengths of the exposing light. Today, 193 nm radiation is used for advanced circuits. To obtain smaller, sub-wavelength features, complex structures are used on the masks, increasing the mask cost significantly. Using shorter wavelengths to continue the progression to finer features is difficult, however; the materials used for lenses do not readily transmit light with shorter wavelengths. Lithography using wavelengths approaching the X-ray regime is being developed; at these wavelengths, however, obtaining light sources with adequate intensity can be limiting.

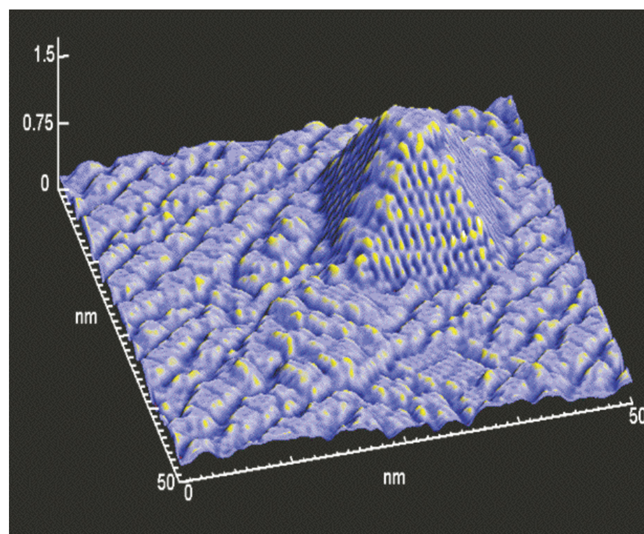
Alternatively, techniques for physically imprinting the features into a polymer layer are being explored.[1,2] A mold is pressed into a soft polymer, and then the polymer is hardened. Such *nanoimprint lithography* is not limited by the wavelength of light and can form features on the order of 10 nm. Many features are formed at the same time, avoiding the serial nature of other advanced techniques. The polymer can be cured either thermally or by ultraviolet light. Although nanoimprint lithography can form very fine features, features of the same size must first be created on the mold. Although the mold can be reused many times, it is generally built using expensive electron-beam lithography. Fine lines and spaces can be defined with a mold made from the edge of a differentially etched stack of layers, but the technique is expensive and limited to specific patterns.

Bottom-Up Fabrication

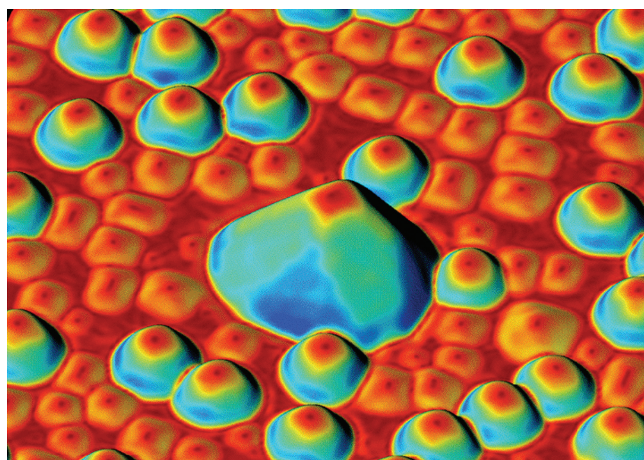
Although great progress continues to be made in pattern definition by these top-down approaches, the complexity of the processing, and the associated costs, continue to increase. Today, the physical and economic limitations of conventional and non-conventional top-down technologies are widely recognized, and alternative bottom-up techniques are being considered. In these techniques a basic physical or chemical mechanism is used to form the small features. Generally, the locations and sizes of these features are less predictable than for features formed by deterministic, top-down techniques; therefore, using self-assembled nanostructures requires reconsidering circuits and architectures to accommodate these limitations. Two bottom-up approaches are discussed here: (1) Structures formed by lattice mismatch strain (briefly) and (2) metal-catalyzed nanowires (in more detail).

Strain-Induced Nanostructures

When one crystalline material is deposited on another crystalline material under suitable conditions, the atoms of the depositing material can position themselves above low-energy locations of the substrate (*i.e.*, epitaxially). When the lattice of the deposited material differs from that of the substrate, the strain energy from the lattice mismatch increases as the layer becomes thicker, leading to limits on the thickness of defect-free, two-dimensional layers.



(a)



(b)

Fig. 1. Self-assembled Ge/Si(001) islands formed by lattice mismatch between deposited Ge and the Si substrate. (a) Scanning-tunneling micrograph of 5 equivalent monolayers of Ge, showing the dimers on the pyramid and the rough surface of the Ge wetting layer. (b) Atomic-force micrograph of 11 equivalent monolayers of Ge, showing three different types of Ge islands.[4] (Color enhancement of figures courtesy of G. Medeiros-Ribeiro, LLNS, Brazil, and Hewlett-Packard Laboratories.)

Under suitable conditions, the depositing material can lower its energy by expanding into the third dimension, forming distinct nanostructures. Typically, these three-dimensional structures are surrounded by a two-dimensional *wetting layer* of the material being deposited. If the lattice mismatch is the same in two in-plane directions, the three-dimensional structures are equiaxed islands extending above the wetting layer, as shown in Fig. 1. This geometry is observed for the well-studied Ge/Si(001) system[3,4] and the InAs/GaAs system.[5,6]

When the lattice mismatch, and hence the strain in the system, is anisotropic, the islands are no longer equiaxed, but are narrower in the high-strain direction than in the low-strain direction. The strain is anisotropic for rare-earth silicides on Si; for example, $ErSi_2$ (Fig. 2) and $DySi_2$ on Si(001).[7,8] The nanowires formed on the surface can be very small (*e.g.*, a few nanometers) in one direction and much longer (*e.g.*, hundreds of nanometers) in the orthogonal direction. The structure of the nanowires has been studied by *in situ* scanning-tunneling microscopy.[7,8] Conduction along self-assembled nanowires exhibits quantum effects,[9] and is somewhat lower than in the bulk, presumably limited, at least partially, by surface scattering. Because the nanowires are very thin, their electrical resistance is high, but they can be used as an etch mask to define a thicker, underlying layer, which may have lower resistance. Thus, lattice mismatched systems may be used to form nanowires and islands. However, they require that the underlying material be crystalline, precluding their use for many potential applications.

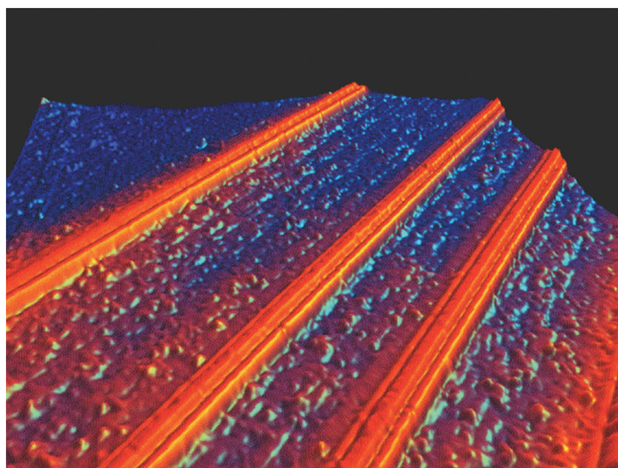


Fig. 2. Scanning tunneling micrograph of $ErSi_2$ on Si(001), showing the elongated structures formed because of the anisotropic lattice mismatch between $ErSi_2$ and the Si substrate.[7]

Metal-Catalyzed Nanowires

An alternative method of forming self-assembled nanowires offers more possibilities for integration. Briefly, nanowires are grown by interaction of a depositing material with a catalyst nanoparticle. Typically, metal catalyst nanoparticles are first formed on a substrate. The material used to grow the nanowires (often a semiconductor) is then transported to the nanoparticles. Atoms of the nanowire material precipitate preferentially between the nanoparticles and the substrate, pushing the nanoparticles away from the substrate and forming columns of material (*i.e.*, nanowires) of approximately the same diameter as the nanoparticles. These processes are discussed further below.

The nanoparticles are often formed by depositing a very thin (≤1 nm) metal layer on a substrate and then annealing at an elevated temperature. Because the layer is very thin, surface energy causes the layer to agglomerate into isolated nanoparticles, with the size of the nanoparticles being influenced by the annealing conditions. Alternatively, preformed metal nanoparticles in a colloidal suspension or in the gas phase can be deposited directly on the substrate.

Several different techniques can be used to supply the nanowire material; we focus our discussion on chemical vapor deposition (CVD) of Si. The substrate with metal nanoparticles is exposed at an elevated temperature to a gas containing Si under conditions where Si does not normally deposit. The catalyst nanoparticles accelerate the decomposition of the Si-containing gas so that Si atoms and by-product atoms form on the surface of the nanoparticles. The by-products then desorb into the gas phase. (Under conditions typically used for nanowire growth, the uncatalyzed deposition of Si is often limited by desorption of the reaction by-products, so the catalyst probably promotes the reaction by aiding desorption of the by-product.) The Si diffuses through or around the nanoparticles and precipitates between the nanoparticles and the substrate, forming the nanowires.

The catalyst nanoparticles can be either in the liquid or the solid phase during nanowire growth. The former is more common, and nanowire growth by this *vapor-liquid-solid* process has been well known (albeit at larger dimensions) for several decades.[10,11] More recently it was extended to the nanoscale.[12-14] Gold is a typical catalyst. The Au-Si eutectic temperature is about 360°C, and Si nanowire growth typically occurs at about 600°C, so the nanoparticles are in the liquid form during nanowire growth. Ti is also a suitable catalyst for nanowire formation. The lowest eutectic temperature of the Ti-Si system is above 1300°C. Even with moderate reduction of the eutectic temperature because of the small size of the nanoparticles, the Ti nanoparticles are probably in the solid phase during nanowire growth. Si nanowires also grow on other selected silicide-forming metals, such as Pt, Pd, and Ni.[15]

Choice of the appropriate catalyst material is strongly influenced by the intended use of the nanowires. Many metals introduce deep energy levels within the Si bandgap. For Au the deep levels are close to the middle of the bandgap, increasing carrier generation and recombination rates (Shockley-Read-Hall recombination)[16] significantly.

The nanowire diameters are similar to those of the catalyzing nanoparticles, so control of the nanoparticles is critical in determining the nanowire diameters. In addition, the ratio of catalyzed to uncatalyzed Si deposition should be large to minimize uncatalyzed deposition on the sides of the nanowires, which causes the nanowires to be tapered, rather than cylindrical. This ratio can be increased by controlling the gas-phase species when CVD is used. Either a less reactive Si-containing gas, such as SiH_2Cl_2 or $SiCl_4$, may be used, or gaseous HCl may be added to a H_2/SiH_4 gas mixture. Cl greatly suppresses the uncatalyzed deposition rate on the Si sides of the nanowires, while only moderately decreasing the axial growth rate;[17] nanowires as thin as 6 nm have been grown, approaching the range where the Si bandgap starts to increase with decreasing physical size of the structure, and quantization effects become noticeable.

The nanowires often grow along <111> directions. When single-crystal Si is used as the substrate, the nanowires are often aligned epitaxially and grow along the <111> directions of the substrate. When the technologically important Si(001) orientation is used (Fig. 3a), the nanowires grow in four equivalent directions at about 55° from the substrate normal. When Si(111) is used

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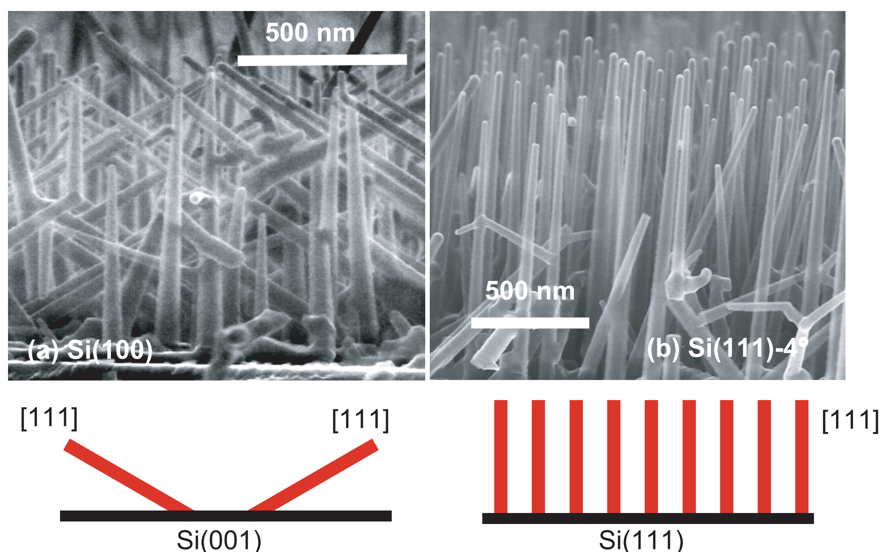


FIG. 3. Ge nanowires on Si showing preferential growth along <111> directions of the Si substrate (a) on Si(001), with the <111> directions at 54.7° from the substrate normal and (b) on Si(111)-4°, with the <111> directions nearly normal to the substrate.[19]

(Fig. 3b), the nanowires can grow nearly perpendicular to the substrate, as is critical in selected applications. Usually, for electronic applications dopant atoms must be added to the nanowire. When CVD is used, the dopant can be added conveniently and effectively from a gas-phase species during nanowire growth.

In addition to Si, Ge nanowires and nanowires of other materials may also be grown by similar techniques; however, Si nanowires often form more readily. The catalysts useful for growing Ge nanowires are much more limited, with reported work focusing almost exclusively on Au.[18,19] In addition to nanowires formed by a single semiconducting material, heterostructures can be formed by depositing different semiconductors sequentially.[20,21] If deposition of both semiconductors is catalyzed by the metal nanoparticles, regions of different materials can be sequentially grown in the axial direction, creating heterojunctions between the adjacent segments. These heterostructures can be especially useful in optically active structures made from compound semiconductors, where some segments along the length of the nanowire are light emitting and others are not. Alternatively, the first semiconductor can be formed by metal-catalyzed deposition, and the second by uncatalyzed deposition on the side surfaces of the first semiconductor to create *core-shell* nanowires.[22] The band offsets can be used to selectively control the location of carriers.

Applications of Metal-Catalyzed Nanowires

One major limitation of conventional electronics is interconnecting the active electronic elements. Both nanowires and carbon nanotubes have been proposed as the vertical interconnecting elements. For this application, process compatibility is critical because the nanostructures probably need to be grown at specific locations on the partially fabricated underlying circuit. Alternatively, preformed nanostructures can be placed on the circuit to serve as interconnections.

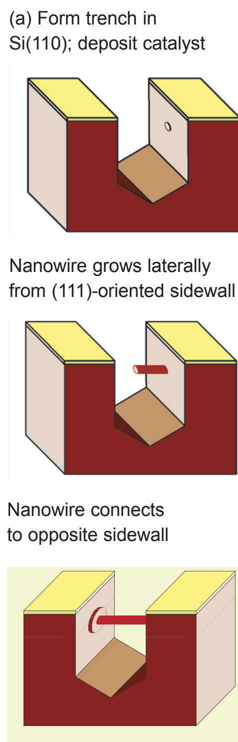
Because of their small diameter and controlled electrical properties, nanowires may serve as the channels of field-effect devices, in which the conductance of the nanowires is modulated by an external electric field perpendicular to the nanowire axis. The device can be a field-effect transistor, with the field created by a gate electrode placed on the surface of an insulating layer. If the gate electrode is omitted, the conductance is sensitive to charge near the surface of the nanowire. With a selective coating on the nanowire that interacts only with selected species, the device can become an efficient nanosensor.

For devices that rely on current flow through the nanowires, good electrical connections must be made to both ends of the nanowires. When the nanowires are grown on a substrate, low-resistance connections form between the nanowires and the substrate during growth. Contacting the other end of the nanowires is less straightforward. However, connections can be made by first forming electrodes bounded by vertical (111) planes by anisotropic wet etching of a Si(110) layer[23] and then growing the nanowires from the side of one electrode laterally across the gap toward the (111) surface of the second electrode.[24] When the nanowires impinge on the opposing surface, they bond to it, as shown in Fig. 4, forming good mechanical and electrical connections. The conductivity of the nanowires can be controlled by changing the gas-phase dopant concentration during growth. High-resolution transmission electron microscopy provides further evidence of the high-quality contacts between the grown nanowires and the electrodes on which they impinge during nanowire growth.[25]

In any field-effect device that depends on depletion of mobile carriers to modulate the conductance of a nanowire, there are interrelated constraints on the diameter and doping of the nanowire. If either is too high, the entire diameter cannot be depleted of mobile carriers. The limited thickness of the depletion region sets an upper bound on the dopant concentration for a given nanowire diameter. If unmodulated portions of the nanowire are to be used as interconnections between active elements, however, a high conductance is needed. Thus, a tradeoff must be made between the ability to modulate the conductance of the nanowire and the interconnection resistance. For the maximum dopant concentration that can be depleted, the resistance of a nanowire is on the order of 100 kΩ for a 1 μm length of nanowire. This high resistance can limit the switching speed of devices that must be charged through the nanowire.

Nanowire transistors made from Si have been considered in most detail, but transistors made from Ge nanowires have also been demonstrated.[26] In these Ge devices, the poor quality native oxide on the surface of the Ge nanowire is removed and replaced by a high-permittivity dielectric formed by atomic-layer CVD.

Self-assembled nanostructures offer a potential route to mitigate the physical and economic limits of conventional top-down fabrication. Combining these bottom-up approaches with the extensively developed top-down approaches may extend Moore's law of exponential-



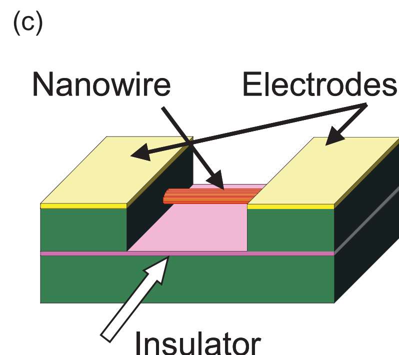


FIG. 4. (a) Schematic diagrams and (b) scanning electron micrograph of bridging nanowires growing laterally across a trench etched into a Si(110) substrate and bounded by Si(111) planes.[24] The nanowires make mechanical and electrical connection when they impinge on the opposing wall of the trench. (c) Schematic diagram of an electrically isolated structure built with bridging nanowires.

ly increasing functionality beyond that currently envisioned. Strain-induced nanostructures and metal-catalyzed nanowires are two approaches to self-assembly, with the latter offering a better-defined path toward process integration and applications.

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