Wafer Bonding: A Flexible Approach to Materials Integration

by U. Gösele and M. Alexe

Wafer bonding, also termed direct bonding or fusion bonding, has increasingly become a technology of choice for materials integration in various areas of microelectronics, optoelectronics, and microelectromechanical systems (MEMS). The Electrochemical Society has played an important role in furthering this new technology by organizing a biannual series of symposia on this subject starting in 1991. In the present article we will describe the status of this technology, and mention major accomplishments as well as challenges and opportunities for future research and applications. We will concentrate on the basic principles involved, rather than on detailed descriptions of applications. Because the literature on wafer bonding has become rather extensive, it is not our goal to be exhaustive but rather to stress aspects which are important or just interesting in our own somewhat personal view. For more details, we refer the reader to the proceedings of the above mentioned conference series,[1,2] a recent book,[3] and a number of excellent review articles on this subject.[4-10] We will cover a range of materials including silicon and III-V compounds, as well as various topics such as low temperature bonding approaches including ultra-high vacuum bonding, thinning processes based on hydrogen-implantation induced layer splitting ("smart-cut" and "smarter-cut"), "compliant universal substrates" based on twist wafer bonding, and the potential use of wafer bonding for the protection of wafer surfaces.

What is Wafer Bonding?

Wafer bonding refers to the phenomenon that mirror-polished, flat and clean wafers of almost any material, when brought into contact at room temperature, are locally attracted to each other by van der Waals forces and adhere or bond to each other. In most, but by far not all cases, the wafers involved in actual applications are typical single crystal semiconductors such as silicon or gallium arsenide. After starting the bonding process, by locally applying a slight pressure to the wafer pair, the bonded area spreads laterally over the whole wafer area in a few seconds as shown in Fig. 1. Because the bonding achieved at room temperature is typically relatively weak, room-temperature bonded wafer pairs usually have to undergo a heat treatment to strengthen the bonds across the bonding interface. Frequently, one of the wafers is then thinned to a thickness in the range of a few nanometers to many micrometers, depending on the specific application. Also depending on the specific application and materials system, the generic process flow as shown in Fig. 2 may be modified in a number of ways

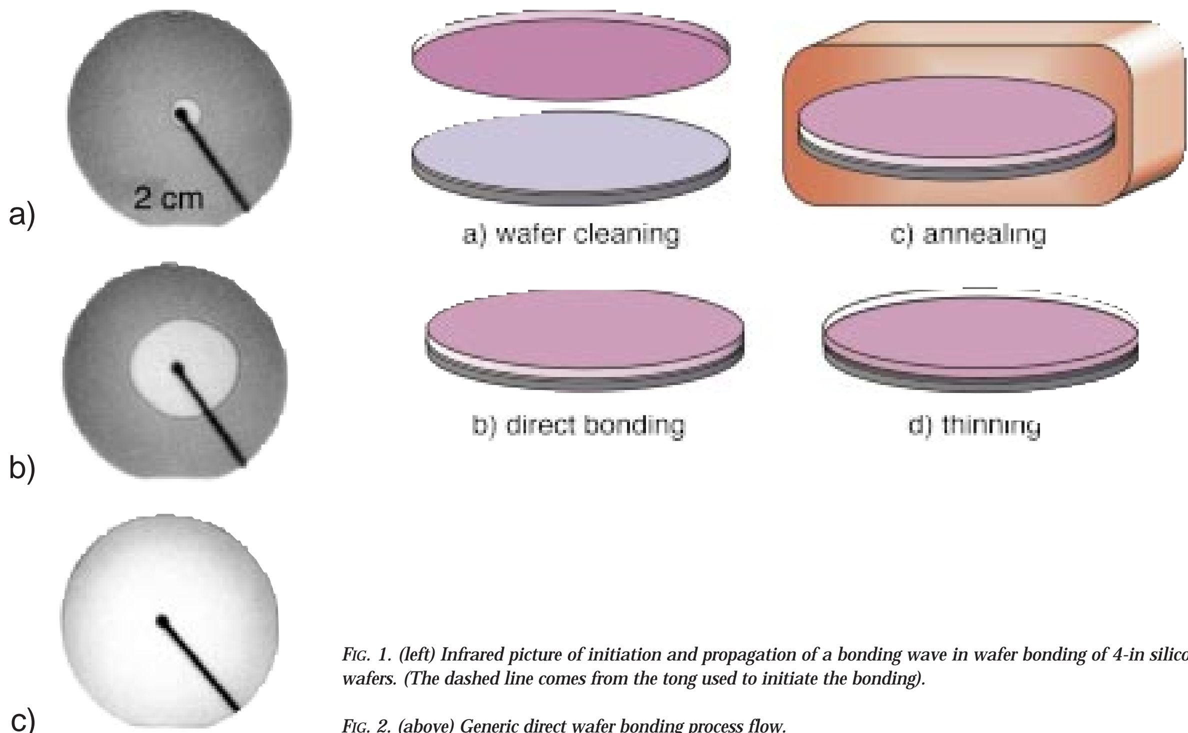


Fig. 1. (left) Infrared picture of initiation and propagation of a bonding wave in wafer bonding of 4-in silicon wafers. (The dashed line comes from the tong used to initiate the bonding).

Fig. 2. (above) Generic direct wafer bonding process flow.

(*e.g.,* no heating or thinning step, combination of the heating and bonding steps, use of an intermediate bonding layer, or of structured wafers).

Historical Background

Probably the first report on the sticking of flat glass plates can be found in a 1638 book by Galileo Galilei.[11] Later on, this phenomenon was empirically known and partly used for optically polished pieces of materials and was first scientifically investigated for polished pieces of quartz glass by Lord Rayleigh in 1936. In the sixties and seventies this adherence phenomenon was used for some isolated applications involving glass or III-V compound wafers. In the eighties, almost simultaneously, researchers at Toshiba[12] and IBM[13] used this room temperature adhesion phenomenon followed by an appropriate heating step to replace the epitaxial growth of thick silicon wafers or to fabricate silicon-on-insulator (SOI) structures, respectively. In the case of SOI wafers, at least one of the silicon wafers is thermally oxidized before bonding so that this oxide layer may later form the required insulating layer. Shortly afterward, bonding of structured silicon wafers was applied for the fabrication of micromachined pressure sensors and termed silicon fusion bonding.[14] In the meantime, wafer bonding has been applied to all kinds of materials combinations involving silicon or other materials. The wide availability of chemical mechanical polishing (CMP) in integrated circuit fabrication and of a variety of precision thinning approaches has led to a widespread and diverse use of wafer bonding. The application areas range from microelectronic devices based on SOI structures, power devices, high voltage devices, optoelectronic devices based on III-V compounds, non-linear optics devices, and MEMS including pressure and acceleration sensors. Although wafer bonding can be applied as a simple and elegant method to join equal or different materials, one of its main advantages appears to be the possibility to fabricate single crystal layers on top of substrates which may be either amorphous, polycrystalline, or a single crystal with large lattice mismatch. The term wafer bonding somehow implies that wafers are involved, but bulk pieces (such as pieces of laser crystals) can also be easily bonded by the same approach provided that the surfaces are sufficiently flat.

Surface Requirements

In contrast to conventional diffusion bonding performed at temperatures close to the melting point, no macroscopic diffusional transport of the materials to be bonded usually occurs across the interface of bonded wafers. Plastic deformation of the wafers also should generally be avoided. As a consequence, wafer bonding requires clean and mirror-polished surfaces that might be chemically conditioned before bonding. The wafers do not have to be atomically flat and may thus contain surface steps and terraces as long as their density is not too high. Because the wafers can deform elastically, a certain waviness and bow can be tolerated. It is nowadays possible to calculate which surface roughness, waviness and bow (as *e.g.* determined by measurements) will still allow bonding for a specific surface interaction.[3] It is fair to say that almost all materials may be polished in such a way that the surface requirements for bonding are fulfilled. Generally, most commercial semiconductor wafers (with the possible exception of SiC) may easily be bonded without further polishing, independent of their diameter and thickness.

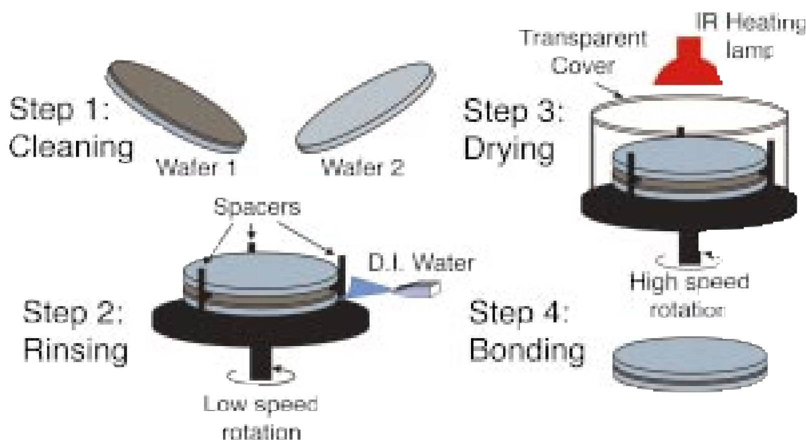


FIG. 3. Schematic of the microcleanroom setup and procedure.

In the best investigated case of silicon wafer bonding, three different kinds of surface conditioning are presently used: (1) hydrophilic surfaces, which usually consist of an oxide layer (native oxide or thermally grown oxide) to which water molecules are attached via intermediate OH-groups; (2) hydrophobic surfaces, which consist of hydrogen saturated silicon surfaces obtained by an HF-dip removing any oxide layer; and (3) clean silicon surfaces without adsorbates, which may be realized only under ultrahigh vacuum (UHV) conditions. For each materials system, the surface preparation step has to be carefully considered especially because the resulting surface layer, even if it consists of only a monolayer, may cause undesirable interface reactions during a heating step.

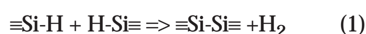
It is worth remembering that cavities in the wafer surfaces do not prevent bonding, whereas particles or local protrusions do prevent bonding at least locally around these disturbances and lead to unbonded areas that are frequently termed interface bubbles. Therefore, particles on the surfaces have to be avoided by proper cleaning and bonding procedures. Surfaces with undesirable surface topographies may be rendered bondable by directly polishing the surface. If this is not allowed or possible, a process and device-compatible sacrifial layer (*e. g.,* a CVD oxide or polysilicon layer or a spin-on glass) may be deposited, which can then be polished to offer a bondable surface.

How is Bonding Performed?

Different bonding procedures appear to be appropriate for different materials systems. Whereas for bonding of hydrophobic and hydrophilic silicon wafers, the actual contact of the two wafers is usually performed at room temperature in ambient atmosphere, bonding of III-V compounds is frequently performed at elevated temperatures in a hydrogen atmosphere. To avoid particles between the wafer surfaces, which would lead to unbonded areas, the contact has to be performed in a clean room of class 10 or better or in a "microcleanroom." A microcleanroom[15] is a centrifuge-based device specifically designed to avoid particles between the wafer surfaces to be bonded (Fig. 3). After contacting the wafers, the actual bonding starts at one location, typically after initiation by local application of a slight pressure. The bonded area then spreads over the whole area within a few seconds as mentioned above and shown in Fig. 1.

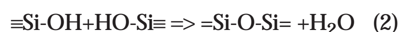
Directly after room temperature bonding, the adhesion between the two wafers is determined by van der Waals interactions or hydrogen bonds and is one or two orders of magnitude lower than typical for covalent bonding. The surface energy is typically around 100 mJ/m^2 for hydrophilic surfaces and around 20 mJ/m^2 for (hydrogen covered) hydrophobic silicon surfaces generated by an HF dip. For most practical applications a higher bond energy is required than obtained after room temperature hydrophilic or hydrophobic bonding. Such an increase (to about 2000 mJ/m^2 for covalent bonding) may be accomplished by an appropriate heating step. In the case of silicon the heating step is associated with chemical reactions. This heating step is frequently performed at temperatures as high as 1100°C in the case of silicon. The reactions at the bonding interface may conveniently be investigated by multiple internal reflection spectroscopy (MIRS).

For details the reader is referred to the literature.[16] For hydrophobically bonded wafers during heating the reaction consists of sequential hydrogen desorption and silicon-silicon covalent bond formation across the interface



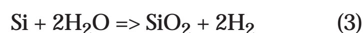
$$\equiv Si\text{-}H + H\text{-}Si\equiv \Rightarrow \equiv Si\text{-}Si\equiv + H_2 \quad (1)$$

At temperatures up to about 600°C the hydrogen does not diffuse into the silicon but rather diffuses along the bonding interface. In the case of hydrophilic wafer bonding, the end result, namely the generation of molecular hydrogen, is the same but there are intermediate steps involved. Initially there exists molecular water at the interface in terms of monolayers of water adsorbed on hydrophilic oxides. Molecular water will also come partly from the reaction



$$\equiv Si\text{-}OH + HO\text{-}Si\equiv \Rightarrow =Si\text{-}O\text{-}Si= + H_2O \quad (2)$$

which starts to form strong covalent bonds across the bonding interface at temperatures above about 120°C. Molecular water will oxidize the surrounding crystalline silicon and form molecular hydrogen via the reaction



$$Si + 2H_2O \Rightarrow SiO_2 + 2H_2 \quad (3)$$

Hydrogen molecules resulting from Reaction 3 cannot appreciably dissolve in the silicon phase and therefore generate a high gas pressure at the interface. This pressure, which may lead to formation of interface bubbles or weakening of the bonding, decreases with increasing oxide thickness (because the hydrogen can be dissolved in the oxide). Therefore, for strong and high quality bonding a combination of a very thin oxide (which favors getting rid of the water via Reaction 3) and a thick oxide (which reduces the pressure at the interface) appears to be most favorable, as indeed was found experimentally.

As mentioned above, the bonding of III-V compounds is frequently performed in a hydrogen atmosphere at elevated temperatures (around 500-650°C) for relatively small pieces of say 1 cm x 1 cm which are pressed together by an external load. Only recently, we managed to demonstrate that whole GaAs wafers of up to 6" in diameter may be bonded in a hydrogen atmosphere without the application of any weights.[17,18] One essential feature of our process is the separation of the two GaAs wafers during heating in hydrogen and the subsequent *in situ* contact of the wafers in hydrogen at elevated temperatures. This procedure should allow wafer based fabrication of bonded vertical cavity surface emitting lasers (VCSELs).

Low Temperature Bonding Approaches

In many cases, in order to avoid thermal stresses or damage to already existing structures in or on the wafers involved, it is desirable to perform wafer bonding close to room temperature or at least at moderate temperatures of only a few hundred degrees centigrade (often termed low temperature wafer bonding). In the case of hydrophilic silicon bonding long-time annealing (for 10-100 hours) at temperatures at 200°C or even lower may lead to relatively high bonding energies.[3] A very promising approach for low temperature bonding is based on various plasma treatments of the silicon surfaces, which in some cases allow for high bonding energies already at room temperature,[19] although one has to be careful to avoid plasma related contamination problems.

An attractive possibility to reach the full bonding energy directly at the room temperature bonding step consists in contacting two silicon surfaces free of adsorbates under UHV conditions.[9] Mechanical testing of UHV bonded 4" (100) silicon wafers confirms the covalent nature of the bonding at the interface. Covalent bonding has also been accomplished for 3" GaAs wafers at temperatures around 300°C under UHV conditions after *in situ* cleaning of the surfaces by atomic hydrogen.[20] The electrical properties of such bonded interfaces are still not yet understood in any detail although they will be important for device applications in which current has to flow across the interface.

Thinning Approaches

Depending on the specific application, frequently thinning one of the bonded wafers down to a thickness between about 10 nm to some micrometers is required. From the many different approaches such as precision polishing, the use of etch-stop or polishing/grinding stop layers (including the remarkable case of a porous silicon layer), we will discuss here only an especially elegant procedure that has been suggested by Bruel and termed "smart-cut."[21,22] It is based on hydrogen implantation before bonding, which leads to the splitting of silicon wafers along hydrogen-filled microcracks induced by the precipitation of the implanted hydrogen during a heating step after bonding (Fig. 4). The process is also known as hydrogen-implantation

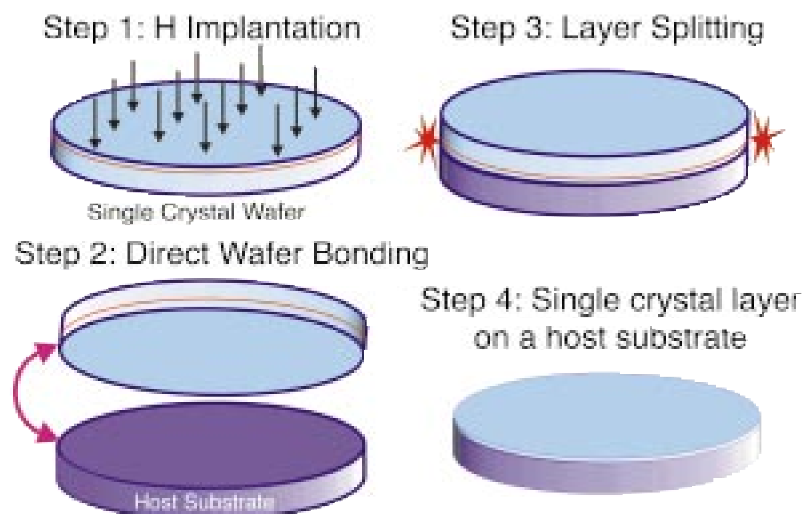


FIG. 4. Schematic of the hydrogen-induced layer transfer.

induced layer splitting, exfoliation, delamination, or ion-cut.

One main advantage of this procedure, which allows a thickness variation in the 10 nm range, is that split wafers may be re-used (after some soft polishing, which is also required for the transferred layer) since its thickness has changed only by about a micrometer or less. Co-implantation of a much lower dose of boron facilitates a decrease of the temperature and/or time of splitting considerably ("smarter-cut").[23] Lower temperature layer splitting is most important for bonding materials with different coefficients of thermal expansion such as silicon and quartz glass. Implantation of silicon at temperatures higher than ambient may lead to fewer defects and will also allow splitting at lower temperatures. Recently it has been demonstrated that hydrogen-implanted wafers may also be split by mechanical means at room temperature instead of using an annealing step causing a gas pressure in the microcracks.[24]

If hydrogen-implanted wafers are annealed without bonding, surface blisters will develop. These blisters will finally break and flaking will occur, which for many years has been known as an undesirable side effect of hydrogen (or helium) implantation. Observing these surface blisters is a convenient way of investigating the hydrogen agglomeration process as a function of implantation temperature, implantation dose and energy, annealing temperature and time, and crystallographic orientation. Layer splitting by hydrogen implantation and wafer bonding is especially interesting for expensive materials such as single crystal SiC, diamond, GaAs, InP, GaN and a number of complex and expensive oxides for which the smart-cut procedure also works. In Fig. 5, the annealing time to observe surface blisters after hydrogen implantation in Si, SiC, InP, GaAs, and $LaAlO_3$ is shown as a function of reciprocal temperature for a dose of about 5 x 10^{16} cm^{-2} of hydrogen molecules.

It is important to note that microcracks may develop only for certain implantation temperatures which may not include room temperature. For too low a temperature, implantation will generate too much lattice damage to allow sufficient hydrogen agglomeration. For too high a temperature, hydrogen is already mobile during the implantation process and will move out of the implanted region. Some approximate temperature windows for hydrogen implantation are compiled in Table I.[10] GaP and most other materials are expected to be susceptible to the layer splitting process, provided that appropriate processing conditions will be used. Repeated transfer of thin single crystal layers of expensive materials onto appropriate inexpensive substrates (*e.g.,* single crystal SiC onto polycrystalline SiC) could allow a large drop in the price of these materials and consequently to more widespread and economic usage. Hydrogen implantation induced layer splitting may also enable further advances in three-dimensional integration of microelectronic devices and possible integration with opto-electronics.

TABLE I. Approximate temperature windows

Single crystal Material	Temperature Window (°C)
Si	50 to 450
SiC	50 to 900
GaAs	160 to 250
InP	150 to 250
c-cut sapphire	700 to 800
GaN	450 to 275
$LaAlO_3$	250 to 500
$LiNbO_3$	25 to 500

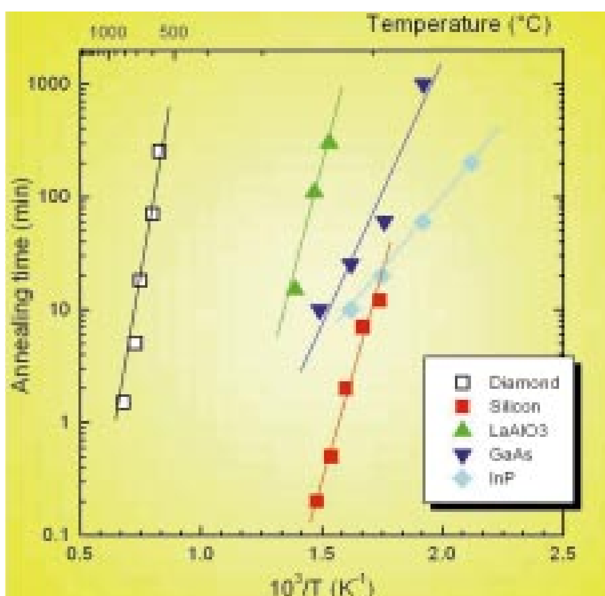


FIG. 5. Blistering time as a function of temperature for different materials.

Compliant Universal Substrates

Heteroepitaxial growth of single crystal layers on a substrate with a different lattice constant leads to the incorporation of misfit dislocations if the film exceeds a critical thickness, which depends on the lattice misfit of the two materials. The generation of misfit dislocations is generally associated with a high density of threading dislocations in the epitaxially grown layer. It has always be a dream to have a "magic" substrate available, which would preclude the generation of misfit dislocations or at least that of threading dislocations.

Theoretically, epitaxial growth on an extremely thin substrate, which would always remain below its critical thickness, has been shown to conform with the growing film such that no misfit dislocation is generated. Although this has also been shown to work experimentally, such thin films as substrates are not practical. Recently, Lo and co-workers[25,26] at Cornell University have fixed a very thin layer of (100) GaAs on a (100) GaAs substrate rotated by a certain twist angle. The fabrication was accomplished by twist wafer bonding of two GaAs wafers one of which contained an epitaxial AlGaAs etch-stop layer followed by a thin (about 3-10 nm) GaAs layer and subsequent back-etching. The resulting structure is schematically shown in Fig. 6. Growth of misfitting III-V compounds (InGaAs and InSb) on this thin GaAs layer bonded on the GaAs handle wafer showed a drastically reduced density of threading dislocations.[25,26] The "compliant universal substrates," as the material was called by Lo and co-workers, has created an enormous interest in the semiconductor community. Presently, it is unclear how such a compliant universal substrate would actually work. In our own experiments, in which we tried to confirm the Cornell results, we also got hetero-epitaxial layers free of threading dislocations[27] but our twist bonded GaAs layer contained a high density of pin holes. In cases where the pin holes were avoided, no dislocation-free heteroepitaxial layers could be accomplished. These results appears to cast serious

doubt on the concept and realization of a universal compliant substrate. Clearly further experiments are desirable in this area.

Surface Protection by Reversible Wafer Bonding

In order to protect the mirror polished surfaces of semiconductor wafers from particle or organic contamination during transport and storage in polymeric boxes, it has been suggested to bond wafers by weak van der Waals bonding and to ship and store bonded wafers instead of single wafers.[28] By this approach, the wafer surfaces would be protected and, in addition, less space would be used for storage and transport resulting in lower costs. The bonded wafers would be separated just before device processing by an air or nitrogen jet as schematically shown in Fig. 7.

What does the Future Hold for Wafer Bonding?

Wafer bonding is now a well established technology for the fabrication of commercially available SOI wafers. This area will become of increasing importance after SOI becomes a mainstream technology. Wafer bonding is also commercially used in the MEMS area. Another commercially established application is the replacement of GaAs substrates by GaP substrates by a wafer bonding process for high efficiency light emitting diodes.[29] In the latter case, as well as in the case of building up smart thyristor structures by bonding two appropriately preprocessed silicon wafers, electrical current has to flow across the bonding interface, a subject which is not yet properly understood.

Wafer bonding may be used for many different areas of materials integration such as three-dimensional photonic crystals,[30] bonding of diamond covered silicon structures for implantable biomedical devices, three-dimensional microelectronic devices (by repeated application of smart-cut procedures), value added substrates (by proper bonding and thinning of GaAs/AlN, GaAs/Si or Si/GaAs), ferroelectric films directly on silicon without the presence of intermediate phases (by a low temperature wafer bonding approach), or magnetoelectronics (by allowing combination of ferromagnetic metals with silicon without the formation of silicides by appropriate bonding procedures), to name just a few. Such possible applications of materials integration are astonishingly diverse and apparently limited more by our lack of imagination than by technological restraints. ■

Acknowledgments

We are indebted to Dr. Q. Y. Tong for his invaluable input during many years of collaboration. We also appreciate the fruitful collaboration with many graduate students, postdoctoral fellows, scientific staff and colleagues at Duke University and the Max Planck Institute in Halle.

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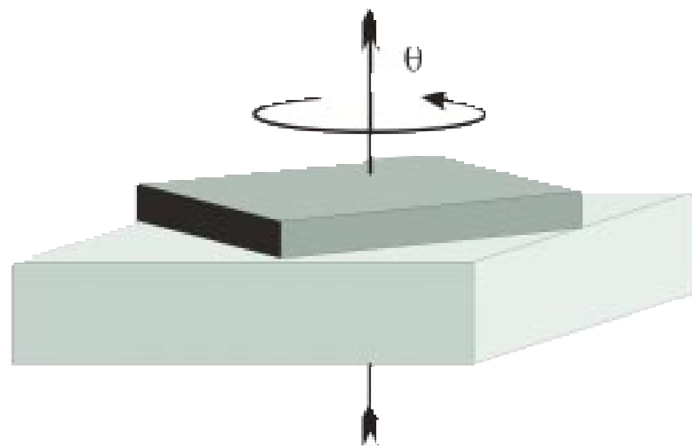

FIG. 6. Schematic of twist-wafer bonding used for fabrication of compliant substrates.

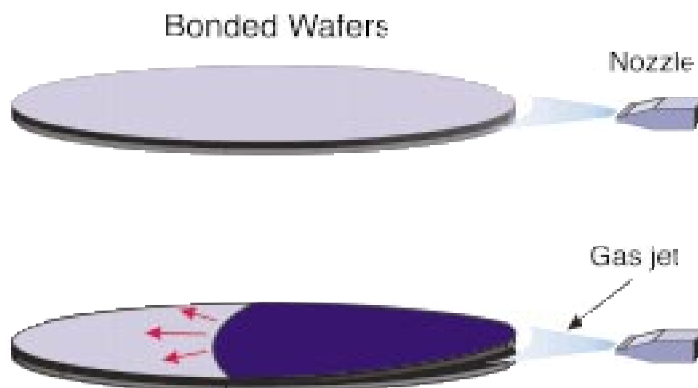

FIG. 7. Step of debonding by gas jet used for surface protection by bonding and debonding (from Ref. 2).

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About the Authors

Ulrich M. Gösele *has been a director at the Max Planck Institute of Microstructure Physics, Halle, Germany since 1993. For many years he was a J. B. Duke Professor of Materials Science at Duke University in North Carolina. His research interests include defects and diffusion processes in semiconductors, quantum effects in porous silicon, self-organized structure formation, photonic crystals and semiconductor wafer bonding. He holds numerous patents on wafer bonding technology and has co-organized various symposia in this field. Together with Prof. Q. Y. Tong he wrote the first book on semiconductor wafer bonding, sponsored by ECS and published by John Wiley & Sons.*

Marin Alexe *is a scientist at the Max Planck Institute of Microstructure Physics, Halle, Germany. After receiving his PhD from the National Institute of Materials Physics, Bucharest, he joined MPI-Halle. His main research interest is in the area of ferroelectric thin films and nanostructures, and materials integration via direct wafer bonding.*