Silicon Complementary Metal-Oxide-Semiconductor Field-Effect Transistor

by M. Tao, R. M. Wallace, C. R. Cleavelin, R. L. Wise

The metal-oxide-semiconductor field-effect transistor (MOSFET or more often MOS) is the most prolific semiconductor device in this information age. Each computer chip contains millions of MOSFETs. Large numbers of MOSFETs are also found in almost all modern consumer products: television sets, cellular phones, automobiles, MP3 players, etc. Commercially mass-produced MOSFETs are manufactured exclusively on silicon (Si), which makes it the most popular semiconductor. A key reason for the dominance of Si is the innate properties of its surface. When it is oxidized to silicon dioxide (SiO_2), the interface between SiO_2 and Si has excellent electrical properties which allow the reliable operation of MOSFETs. No other semiconductors have shown comparable properties and thus they have not been utilized in commercial MOSFETs.

Figure 1a illustrates schematically the structure of an n-channel MOSFET (NMOS), in which electrons serve as the carrier for the electrical current. It is a three-terminal device with three electrodes: gate, source, and drain. When the gate is biased at 0 V, the Si region below the SiO_2 layer is p-type and there are two back-to-back p-n junctions between source and drain. When a voltage is applied between source and drain, the resultant drain current is small due to the two back-to-back p-n junctions. This is the OFF state of the NMOS. If a positive voltage is applied to the gate, negatively charged electrons are attracted to the region below the SiO_2 layer and positively charged holes are repelled from that region. When the voltage reaches a threshold (often called the threshold voltage), the electron concentration in the region exceeds the hole concentration, and a thin layer of the p-type region immediately below the SiO_2 layer turns into an n-type region. This converts the two back-to-back p-n junctions into a continuous n-type channel region. If at this time a voltage is applied between source and drain, a large drain current will flow through the channel. This is the ON state of the NMOS. Therefore, the voltage applied to the gate modulates the current through the channel, resulting in a fast switch between ON and OFF states. Figure 1b shows the current-voltage relation for a typical NMOS with a threshold voltage of ~2 V.

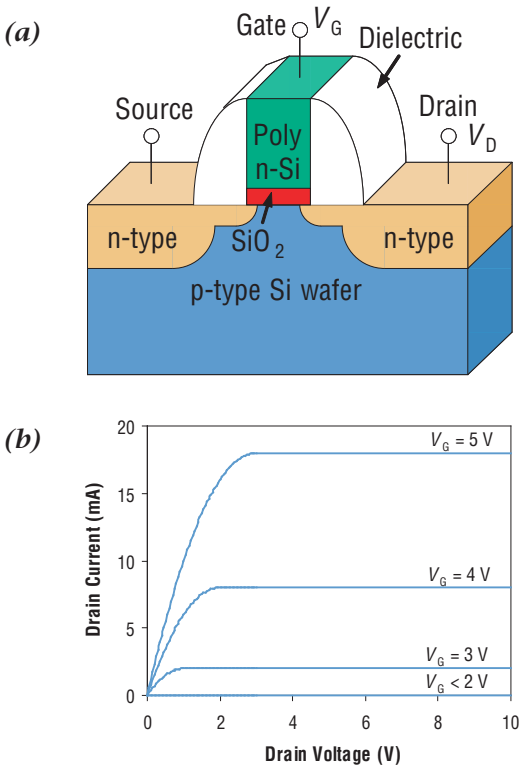

FIG 1. (a) Schematic of a planar silicon NMOS. (b) Current-voltage relation for a typical NMOS with a threshold voltage of ~2 V.

Jack Kilby's invention of the integrated circuit in 1958[1] made possible the integration of many MOSFETs, resistors, capacitors, and other components into functional circuits on a single silicon chip. The functionality of the chip depends largely on the number of MOSFETs integrated. Nowadays, state-of-the-art semiconductor technology can integrate over a billion MOSFETs onto a chip the size of one's thumbnail.

When so many MOSFETs are integrated together, power dissipation becomes a critical issue. Although each MOSFET consumes only a few microwatts of power, millions of these integrated devices dissipate several hundred watts of heat on a thumbnail-sized chip. For this reason, an NMOS is almost always paired with a PMOS, *i.e.*, a p-channel MOSFET in which holes serve as the current carrier. This technology is called complementary MOS or CMOS, and has the lowest power dissipation among all the microelectronic devices currently known. Figure 2a illustrates schematically the structure of a CMOS inverter. The input voltage (V_{IN}) is applied to both gates of the NMOS and PMOS. A positive voltage (V_{DD}) is applied to the drain of the PMOS, and the source of the NMOS is grounded. The source of the PMOS and the drain of the NMOS are connected to the output (V_{OUT}). The operation of this CMOS inverter is as follows: when V_{IN} is low at ~0 V, the output is high at ~V_{DD}. When V_{IN} is high at ~V_{DD}, V_{OUT} becomes low at ~0 V.

In digital applications such as computing and telecommunication, the CMOS inverter serves as the basic logic block with two states, 0 and 1, which correspond to the high and low states of the CMOS inverter, respectively. Therefore, when the input is 0, the output is 1. When the input is 1, the output is 0.

A significant feature of this CMOS inverter is that it does not consume power when it is locked in a particular logic state, either 0 or 1. The only time it consumes power is when it switches from logic 0 to 1 or vice versa. Figure 2b shows its supply current, *i.e.*, the drain current of the PMOS, as a function of input voltage. There is no current when V_{IN} is either high or low. The maximum current is drawn when V_{IN} is between high and low (2-3 V for this particular CMOS inverter).

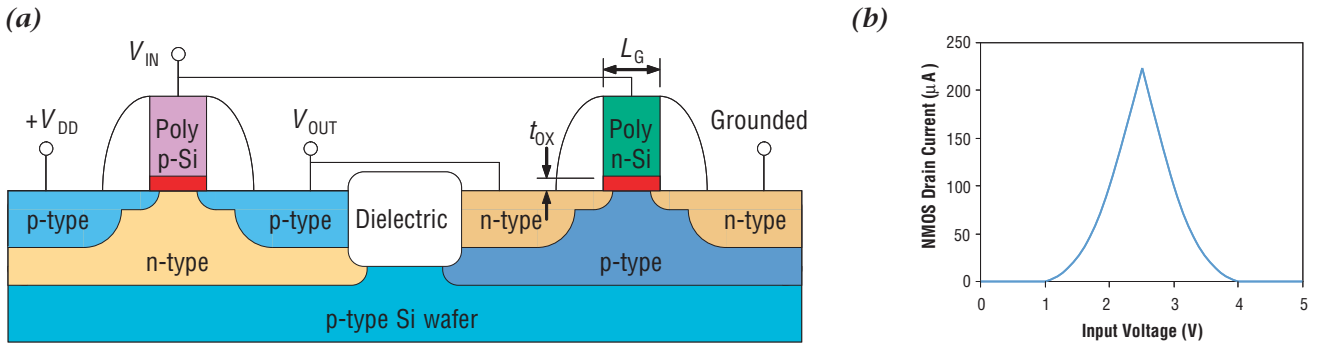

FIG. 2. (a) Schematic of a CMOS inverter, which consists of an NMOS (right) and a PMOS (left). (b) Supply current for a typical CMOS inverter vs. *input voltage.*

The phenomenal progress of the semiconductor industry in the last four decades has been driven mainly by reducing the size of integrated CMOS devices, which can be gauged by the gate length L_G in Fig. 2a. When CMOS devices shrink, more devices can be integrated onto a chip, the functionality of the chip improves, and the cost-per-function drops. This is the famous observation known as Moore's law.[2] Figure 3 shows the number of MOSFETs integrated on a chip over the last four decades.[3] In 1971, about 2,000 MOSFETs were integrated on Intel's 4004 chip, but today over a billion MOSFETs can be integrated on an advanced chip. The gate length of the MOSFETs on Intel's 4004 was ~10 μm, and now it is less than 50 nm and still shrinking. The societal impact of Moore's law is significant. Its economics has brought integrated circuits into every aspect of our life through computing, telecommunication, and other consumer electronics.

However, future progress of the CMOS technology is encountering serious roadblocks. An example is the SiO_2 layer in Fig. 2a. Its thickness (t_{OX}) must be reduced in proportion to the decrease in gate length L_G for the gate to continue to modulate the current through the channel. In the most advanced CMOS devices, it is only a few angstroms (*i.e.*, a few atomic layers) thick. Due to quantum tunneling, a dielectric of such thickness no longer behaves like an insulator, and substantial leakage current flows through it. To suppress this leakage current, researchers are searching for an alternative dielectric with a higher dielectric constant which allows a thicker dielectric to replace SiO_2, the so-called high-*k* dielectric. Additional challenges for future MOSFETs include low-resistance contacts to source and drain, a metallic material for gate, and addition of germanium to the channel region for faster carrier movement. More complicated device structures are also under consideration. For more information on the future of the CMOS technology, the reader is referred to the spring issue of *Interface* and the *International Technology Roadmap for Semiconductors*.[4] ■

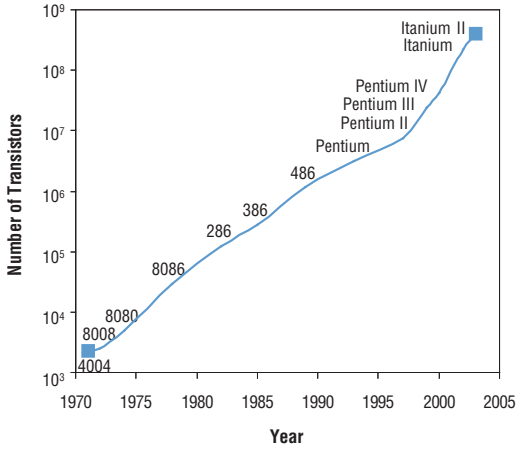

FIG. 3. Number of MOSFETs integrated on a single silicon chip over the last four decades.

References

1. U.S. Pat. 3,138,745 (1959).
2. G. E. Moore, *Electronics*, **38** (April 19, 1965). Also see *Interface*, Spring 2005.
3. http://www.intel.com/research/silicon/mooreslaw.htm.
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