An Update on Low-*k* Dielectrics

by Stephen Beaudoin, Shaun Graham, Ravi Jaiswal, Caitlin Kilroy, Brum Soo Kim, Gautam Kumar, and Shanna Smith

To meet increasingly demanding performance requirements, the microelectronics industry is required to deliver new technology solutions that will include new device architectures, ever-smaller feature dimensions, new high-performance materials, and novel processing schemes. In interconnects, resistance-capacitance (RC) time delays must be properly managed for gains in device performance to be realized. The demands on interconnect performance are most significant in processors. In its description of the 10 most difficult interconnect challenges, the 2004 update to the *International Technology Roadmap for Semiconductors (ITRS)* identifies the top three challenges, all of which are coupled tightly to dielectric performance[1]

- Introducing new materials to meet conductivity requirements and to reduce the dielectric permittivity
- Engineering manufacturable interconnect structures compatible with new materials and processes
- Identifying solutions which address global wiring scaling issues

Table I shows the ITRS predictions of dielectric performance in processor applications for current and future technology nodes up to 2009. The technology nodes are defined as the half-pitch width of a dynamic random access memory (DRAM) in nanometers.

For the 45 nm node (2010), the effective dielectric constants for the interlevel dielectrics become 2.3-2.6 and the anticipated bulk values are less than 2.1. The ITRS indicates that no manufacturable solutions exist for the 45 nm node.

Low-*k* Dielectric Options

While SiO_2 met the performance demands of past interlevel dielectrics, lower-*k* dielectrics are required for current and future technology needs. Lower-*k* dielectrics in use today are commonly grouped as either ultralow-*k* ($k < 2.2$-2.4) or low-*k* ($2.4 < k < 3.5$). These materials can be deposited either by a spin-on route (spin-on dielectrics or SODs) or by a chemical vapor deposition (CVD) or plasma-enhanced (PE)CVD route, and their final properties are influenced by both the deposition method and postdeposition treatment steps, such as anneals or chemical treatments.

The SODs are primarily polymers or organically modified SiO_2 (OSGs, or organosilicate glasses), and recent candidates include

- SiLK™ (Dow Chemical)
- FOx HSQ™ and XLK porous HSQ™ (Dow Corning)
- MSQ and HSQ compounds from the EKD and LKD series (JSR)
- MesoELK™ (Air Products)
- Nanoglass 2.0™, CX-3™, FLARE™, and HOSP (Honeywell Electronic Materials)
- Cyclotene™ (Dow Chemical).[2-5]

HSQ is hydrogen silsesquioxane, an interconnected network of $(H\text{-}SiO_{3/2})_n$ units. MSQ is methyl silsesquioxane, an interconnected network of $(CH_3\text{-}SiO_{3/2})_n$ units. Cyclotene™ is comprised of benzocyclobutene, BCB. HOSP is a mix of MSQ and HSQ. Figure 1 shows a schematic of the structure of OSGs, and Fig. 2 shows a schematic of the structures of several low-*k* polymers.[6,7] The low-*k* SODs have well-controlled molecular properties with *k* values ranging from 2.0 to 2.6.[8]

CVD low-*k* materials include Black Diamond™ and Black Diamond II™

Table I. RC time delay and low-*k* dielectric constants for processor interconnects.[1]

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		*hp90*			*hp65*		
Interconnect RC delay (ps) for a 1 mm Cu metal 1 wire (assumes no electron scattering and an effective ρ of 2.2 μΩ-cm)	191	224	284	355	384	477	595
Interconnect RC delay (ps) for a 1 mm Cu intermediate wire (assumes no electron scattering and an effective ρ of 2.2 μΩ-cm)	105	139	182	224	229	288	358
Interconnect RC delay (ps) for a 1 mm Cu minimum pitch global wire (assumes no electron scattering and an effective ρ of 2.2 μΩ-cm)	42	55	69	87	92	112	139
Interlevel metal insulator (minimum expected)-effective dielectric constant *k*	3.3-3.6	3.1-3.6	3.1-3.6	3.1-3.6	2.7-3.0	2.7-3.0	2.7-3.0
Interlevel metal insulator (minimum expected)-bulk dielectric constant *k*	<3.0	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4

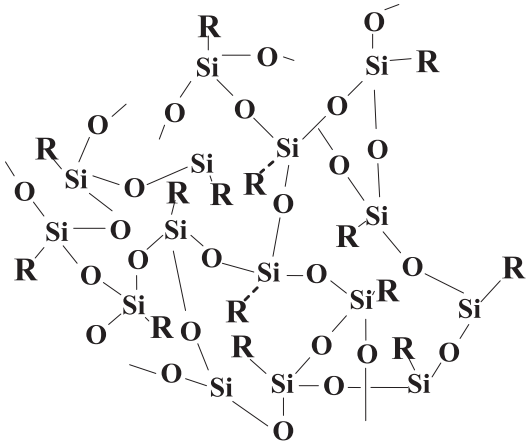

FIG. 1. Schematic representation of OSG structure. In MSQ, R = CH_3; for HSQ, R = H; for FSG, R = F; and for HOSP, R = both CH_3 and H. These compounds can be spin-on or CVD/PECVD dielectrics.

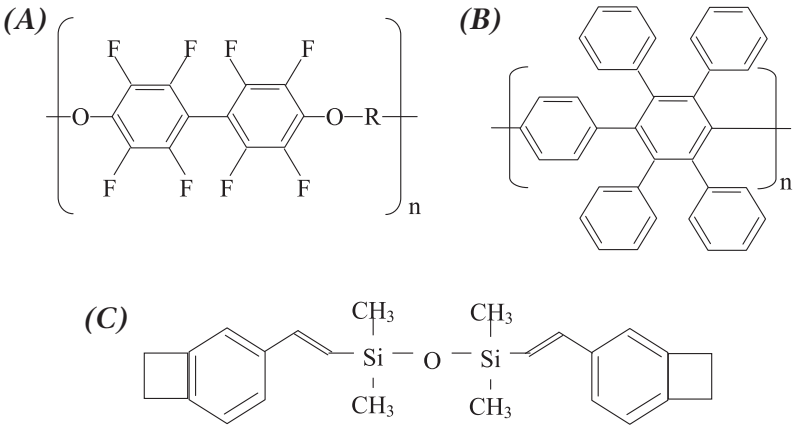

FIG. 2. Schematic of low-k polymers. (A) FLARE™, (B) SiLK™, and (C) Cyclotene™.

(Applied Materials), CORAL™ (Novellus), and Flowfill™ and Orion™ (Trikon).[2,9] These amorphous materials are commonly described as SiCOH, based on a primary silicate (SiO_x) structure with organic species (C_xH_y) that can either be bonded with the silicate or trapped within the silicate structure. Fluorinated silicon dioxide (FSGs, fluorosilicate glasses) PECVD depositions also are practiced.[7,10] Table II shows *k*-values for a variety of low-*k* films.

Imparting porosity to low-*k* dielectrics allows reductions in the *k*-value for these materials. As pores become smaller, the mechanical strength of the layer increases, which is a key consideration for integration and manufacturability.[11] To create porous dielectric films, a sacrificial species can be chemically bonded to the dielectric matrix and later decomposed to form nanometer-scale voids in the low-*k*.[11,12] Alternatively, by judicious choice of precursor and processing conditions, it is possible to deposit dielectric materials that have significant internal porosity at the nanoscale. The pores in low-*k* SODs are typically as large as 20 nm while those in PECVD or CVD materials are closer to 10 nm.[12]

Low-*k* Integration

Effective integration of the new low-*k* dielectrics into manufacturing process flows is a critical challenge facing the adoption of these materials. Because nearly all low-*k* materials will be implemented in a Damascene or dual-Damascene interconnect scheme, the effects of the required patterning, metallization, and chemical mechanical planarization (CMP) on the dielectric performance must be considered. Figure 3 shows schematically the difficulties that can arise when integrating low-*k* materials into interconnect environments. Penetration of Cu into the dielectric is indicated when Cu deposition or CMP is performed in the absence of effective cap/hard mask/etch stop and barrier layers. Others have shown injection of Cu^+ ions into MSQ films.[17] This indicates that cap and barrier layers are necessary to protect these films during metallization processing. It is common to use SiC, SiO_2, or SiOCNH for this purpose.[17-19] Independent of the barrier choice, the effect of the barrier on the overall dielectric properties of the stack must be considered. Generally, the presence of the barrier layer increases the dielectric constant of the layer. The dielectric also must be able to withstand the shearing forces applied during CMP without tearing, cracking, or delaminating.[20] This requires strong adhesion between the dielectric and the barrier, as well as strong cohesion within the dielectric itself.[7,10,15,18] The hardness and elastic modulus of some low-*k* dielectrics is shown in Table III. When the hardness of the dielectric itself is low, the dielectric degrades during CMP, although it has been suggested that the elastic modulus, hardness, adhesion, and fracture toughness all influence the CMP survivability.[15,22,23,26,27] Measurements of the hardness and elastic properties of low-*k* films are complicated by the likelihood that the surface layer on these films is compositionally and mechanically dissimilar from the bulk of the films, and both the film thickness and the nature of the porosity also have important effects on the measured mechanical properties.[26,28] Exposure of the low-*k* films to plasmas has been shown to affect the electrical and mechanical properties of the films, as does chemical modification of the film surfaces.[14,27,29]

Reactive ion etch (RIE) etching and subsequent photoresist strip processes can damage low-*k* dielectrics. Fluorocarbon plasmas, often in the presence of oxygen, are used for plasma etching of low-*k* materials,

Table II. Reported values for low-*k* dielectrics.

Film	*k* range	Deposition method	Reference
FSG	3.2-4.1	PECVD	7, 10, 13, 14
Polyimides	3.1-4.0	Spin-on	7, 13
HSQ	2.5-3.3	Spin-on	7, 10, 13
MSQ	2.0-3.0	Spin-on	7, 10, 13, 15, 16
SiOCH	2.2-3.5	CVD, PECVD	7, 9, 10, 13, 16
BCBs	2.6-2.8	Spin-on	7, 10, 13, 14
Fluorinated polyimides	2.5-2.9	Spin-on	13
Diamond-like carbon	2.7-3.4	PECVD	13
Spin-on organics	2.0-3.2	Spin-on	7, 10, 13, 16, 14

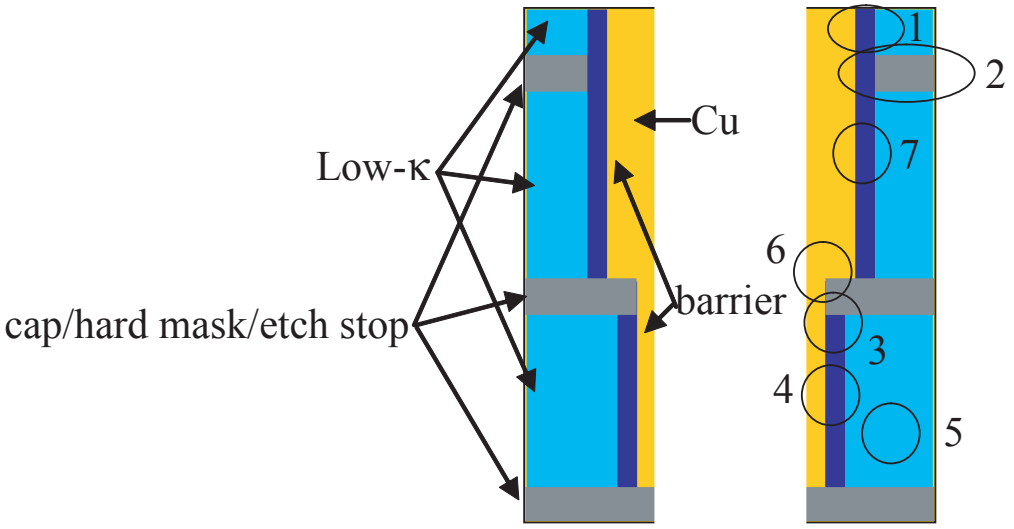

FIG. 3. Schematic of integration issues associated with low-k processing.[15]
1. Damage to dielectric due to RIE and resist strip, difficulty removing etch residues;
2. Inadequate adhesion of cap/etch stop layers to dielectric, delamination during CMP;
3. Inadequate selectivity of etch to low-k vs. etch stop, undercutting of cap/etch stop;
4. Barrier integrity on porous low-k;
5. Inadequate cohesion within low-k;
6. Damage to cap/hard mask/etch stop during bottom etch;
7. Damage during wet and dry cleans after via bottom open etch.

Table III. Reported elastic modules and hardness of low-*k* films.

Dielectric type	Elastic modulus (GPa)	Hardness (GPa)	Reference
Ultralow-*k* OSG SOD	3.78	0.52	21
Ultralow-*k* polymer SOD	4.17	0.16	21
Low-*k* SOD	2.00-14.00	0.40-2.00	22
CVD OSG low-*k*	6.90-14.65	1.30-2.49	21, 23, 26
PECVD CF polymers	> 5.50	> 0.50	24
SiLK (porous)	5.34	0.26	21, 25
SiLK (nonporous)	6.65	0.40	25

and oxygen-based plasmas are desired for postetch resist strip processes. During RIE patterning of CVD SiCOH low-*k* with SiC etch stop, low etch selectivity of the dielectric compared to the SiC leads to premature clearing of the SiC and exposure of the underlying Cu to via etch and wet clean conditions.[15,31] This is most significant during typical overetch processes required to fully clear the dielectric from the via contacts. Subsequent interconnect structures will develop voids beneath the SiC layer, presumably due to the presence of contaminants/damage to the Cu below the SiC layer. Overetch also leads to the formation of sidewall polymers incorporated with Cu that are difficult to remove with standard wet cleans and resist strip processes, as well as corner damage to the cap/hard mask/etch stop on the tops of via openings.[30,31] Generally, there are challenges associated with unfavorable interactions between etch and resist strip processes and the dielectric properties of the low-*k* materials, including preferential removal of hydrocarbon within the dielectrics. Where RIE etching has been performed without altering the C content of CVD low-*k* materials, subsequent plasma resist strip and postetch cleans that remove fluorinated sidewall polymer and photoresist change the electrical properties of the dielectric, including stripping C from the low-*k*.[5,9,15] In other processes, Cl-based plasmas were seen to strip Si from low-*k* films.[5] Supercritical CO_2 with appropriate additives has been used to restore the organic content and dielectric performance of low-*k* films following etching and resist strip.[32]

Cleaning low-*k* dielectrics

Generally, cleaning processes on low-*k* dielectrics may have deleterious effects on the dielectric performance. The porous nature of the low-*k* dielectrics encourages retention of wet cleaning species within the films, which can lead to outgassing difficulties during subsequent processing.[15,33] If amine species enter the pores of the dielectric during the wet clean and outgas during subsequent processing, resist

(continued on next page)

poisoning and inappropriate pattern formation result during lithography. For low-*k* films patterned with fluorocarbons, sidewall polymer may contain C, F, O, and Cu species. Studies of the cleaning of CVD SiCOH dielectrics following fluorocarbon plasma etch revealed that neither reducing plasmas (N_2/H_2), traditional semiaqueous strippers, nor dilute HF cleans were able to remove sidewall polymer residues on low-*k* surfaces when applied individually. Some cleaners that showed promise in the removal of one residue increased the amounts of other residues on the dielectric.[34] In other studies of the removal of fluorocarbon etch residues on CVD SiCOH low-*k*, it was determined that optimized cleans using commercial strippers could remove residues and allow metal interconnections with high electrical yields.[35] The unintended etching of low-*k* dielectrics in cleaning solutions is an issue, although it has been determined that semiaqueous cleans can be optimized to minimize etching.[36] To avoid the interactions between aqueous cleaners and low-*k* dielectrics, cleans in CO_2 have been explored, and the use of supercritical solvents with appropriate additives has allowed for successful cleaning of low-*k* materials.[37,38]

New Low-*k* Materials

The development of new materials and deposition processes to produce low-*k* films remains an area of extreme interest. Various methods have been employed to create these films, including increasing the porosity in existing low-*k* formulations, and using aerogels, xerogels, fluorocarbons, and SiCOH from different precursors.[39-42] Thermal and plasma deposition of fluorocarbon films has produced dielectric layers with *k* values in the range of 2.[42] PECVD of SiCOH films from silane precursors, including trimethyl-, dimethyl-, methyl-, octamethyl, and bis(trimethylsiloxy) methylsilanes have yielded films with *k* values in the range of 2.4-3.2. Siloxane precursors, including 1,1,3,3-tetramethyldisiloxane, octamethyltrisiloxane, and tetravinyltetramethylcyclotetrasiloxane (TVTMCTS), also have been used in PECVD processes to produce low-*k* dielectrics. With the exception of the TVTMCTS, oxygen-bearing plasmas are used, and the work above has focused on tuning of the plasma conditions, including the precursor type, diluent gas, oxygen content, and plasma power, to influence the mechanical and dielectric properties of the resulting films by influencing the porosity of the films, the internal bonding, and the film composition.[43-47] Supercritical fluid deposition of low-*k* films also has been pursued, and films with *k* values as low as 2.0-2.1 have been achieved.[41] As in the low-*k* dielectrics in use currently, challenges remain surrounding the patterning of the dielectrics and their integration into manufacturing.

Conclusions

The 2004 update to the ITRS dictates that demand for interlevel dielectrics with reduced dielectric constants will remain high in the foreseeable future. Current and future materials remain focused on F- and Si-bearing polymers and F-,

C-, and H-doped silicates, most of which involve some level of porosity. Deposition schemes are focused mainly on spin-on, CVD, and PECVD routes, although sol-gel and supercritical CO_2-based deposition options exist. For the candidate dielectrics, the relationships between the methods and precursor types used during film deposition; the resulting film composition, bonding, and porosity; and the mechanical and dielectric properties of the films are still being explored. Integration of the new dielectrics into manufacturable interconnect schemes remains a challenge, and solutions will involve engineering of the films themselves and of the processing schemes to pattern and metallize them. ■

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About the Authors

Stephen P. Beaudoin is Associate Professor of Chemical Engineering at Purdue University. His research interests center on the adhesion of particles and thin films during interface processing and chemical mechanical planarization, as well as interface modification for biological and biosensing applications. He can be reached at sbeaudoi@purdue.edu.

Shaun Graham, Ravi Jaiswal, Caitlin Kilroy, Bum Soo Kim, Gautam Kumar, and Shanna Smith are graduate students in the Department of Chemical Engineering at Purdue University, advised by Stephen P. Beaudoin. E-mail addresses in the same order as above are shaunrg@purdue.edu, rpjaiswa@ecn.purdue.edu, ckilroy@purdue.edu, kim188@ecn.purdue.edu, gautam@purdue.edu, and shannaj@purdue.edu.