Silicon-Based Ultrathin Dielectrics

by R. P. S. Thakur, Y. Chen, E. H. Poindexter, and R. Singh

The phenomenal sustained growth of the electronics industry in the last three decades is primarily due to the success of silicon integrated circuit technology. As compared to any other technology, complementary metal-oxide-silicon (CMOS) transistor based integrated circuits have dominated the field of semiconductor manufacturing. Figure 1 shows the trends in metal-oxide-silicon field effect transistor (MOSFET) parameters with time.[1] As shown in Fig. 1, reduction of channel length (L_g), reduction of power supply (V_{dd}), reduction of gate oxide thickness, and increase of drain current (I_d) are all responsible for the reduction of transistor delay time (t_{pd}). Continued scaling of silicon CMOS toward 100 nm and lower feature size circuits requires effective gate oxide thickness to be below the tunnel dimension of 2-3 nm. From a process integration point of view, development of a perfect gate dielectric process flow in the future CMOS manufacturing sequence is one of the most challenging problems faced by silicon integrated circuit (IC) researchers.

This paper presents details on ultrathin (silicon dioxide and silicon nitride based composite structures) dielectrics that have the potential for meeting future device requirements. In addition to process integration and manufacturing related issues, special emphasis has been placed on the fundamental understanding of the defects both at the interfaces as well as in the bulk of ultrathin dielectrics. The first section deals with the issue of minimum thickness of silicon-based dielectrics. Various approaches being considered to meet future device requirements are addressed next. Fundamental issues dealing with defects and reliability are considered in the next section. The last section deals with process integration and manufacturing considerations.

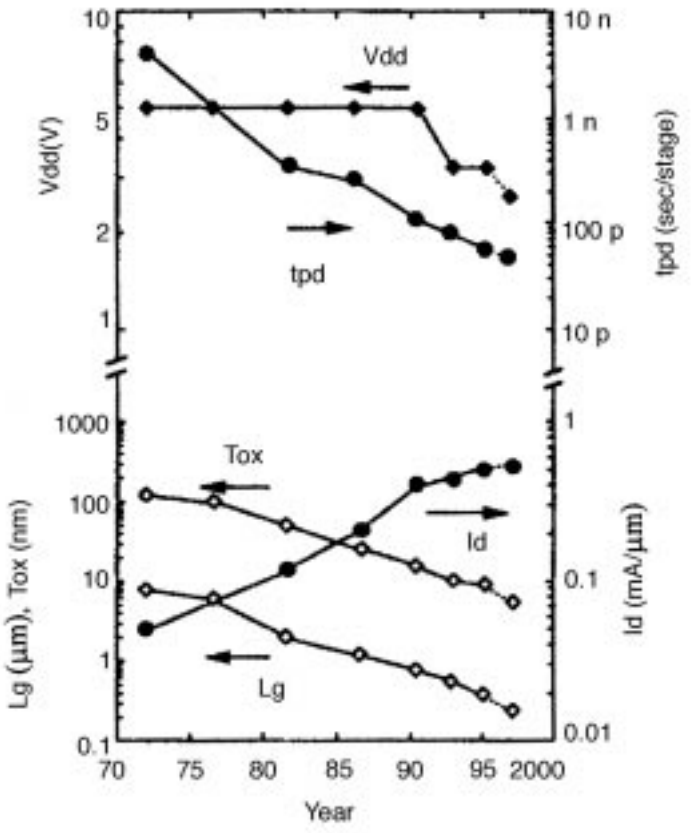

FIG. 1. Trends in MOSFET parameters and characteristics (from Ref. 1).

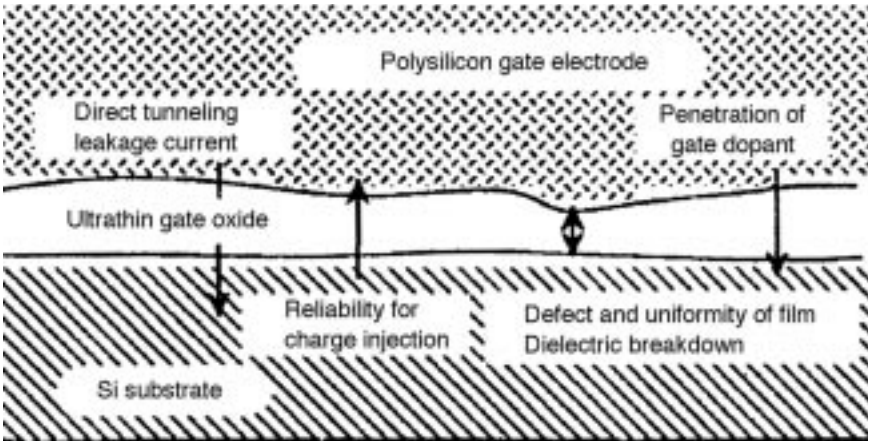

FIG. 2. Concerns in ultrathin gate oxides (from Ref. 1).

Minimum Thickness of Silicon-Based Dielectrics

Even before the current interest in ultrathin gate oxides for MOSFETs had begun, ultrathin 1-2 nm gate oxides have been used in the fabrication of conductor-insulator-semiconductor solar cells.[2] Due to the presence of tunneling leakage currents, the minimum thickness of the gate oxide in MOS transistors was considered to be about 2.8-3.0 nm. However, in 1993, researchers at Toshiba reported the fabrication of 40-nm gate length MOSFET

based on 3-nm gate oxide.[3] In 1994, the same group reported the use of 1.5 nm gate oxide in the fabrication of high performance n-MOSFET.[4] Since the publication of this report, several groups have been working on gate oxides less than 2-nm thick. In a recent publication,[5] the use of 0.7-nm thick silicon dioxide as the gate oxide of MOS integrated circuits has been proposed. In light of the importance of ultrathin silicon based gate dielectrics, it is quite important to establish the lower limit of thickness of gate dielectrics.

As shown in Fig. 2,[1] there are a number of concerns in the use of ultrathin oxides as the gate dielectric. Therefore, in considering the minimum gate dielectric thickness, the problem of significant sub-threshold current has to be taken into account The transistor off current (I_{off}) gives rise to stand-by power consumption:

$$P_{stand\text{-}by} = I_{off} V_{dd}$$

where V_{dd} is the power supply. The stand-by power consumption takes place irrespective of the fact whether the circuit is performing a useful function or not and can be significant compared to the dynamic CMOS power consumption:

$$P_{switching} = f C V_{dd}^{2} / 2 K$$

where f is the clock frequency, C is the total capacitance and K is a factor that can have a value of the order of several tens to hundred.[6] Thus, even for a perfect gate oxide, the stand-by power of an advanced chip containing almost half billion or so transistors, can be significant compared to the switching power of the CMOS circuit. Recently, experimental results on ultrathin oxides have been reviewed.[7] Due to the absence of theoretical or experimental results on small-feature size large-scale circuits based on tunnel oxides, it is not possible to state a single number as the minimum gate oxide thickness. The off currents of a 3 nm and 1.5 nm thick oxides differ by about 4-6 orders of magnitude. Thus, as stated before, due to the stand-by power consumption issue, it is highly unlikely that oxides less than about 1.2 to 1.5 nm thick will ever be used as gate dielectrics. As shown in the companion article in this issue, thick high-k dielectrics can avoid the tunneling current problem.

Silicon-Based Thin Dielectrics

From the consideration of device mobility, generally ultrathin films of silicon dioxide provide the best results. On the other hand, ultrathin films of silicon nitride provide the most effective barrier against diffusion of boron or other elements in the gate oxide. Research in ultrathin gate oxides is proceeding in three different directions. In one approach, the goal is to incorporate nitrogen at the gate/dielectric interface. In the second approach, a metal replaces the poly-silicon gate. In the last type of approach, ultrathin oxide films have been used as the gate dielectric material.

"Control of nanoscale atomic roughness at the Si-SiO_2 interface and structural homogeneity are crucial for the use of silicon-based ultrathin dielectrics as gate dielectric materials in the 21st Century."

The future processing trends are toward single wafer processing. However, this does not mean that conventional batch processing based on thermal furnaces has disappeared. In the case of thermal processing, higher heating and cooling rates as well as mini-batches are being used. Ultrathin silicon based oxides, nitrides, and oxynitrides can be formed by a number of processing techniques. Rapid thermal processing (RTP) based on incoherent light as the source of energy has emerged as an important technique for processing silicon based ultrathin dielectrics.[8,9] Rapid thermal oxidation, rapid thermal chemical vapor deposition (RTCVD), rapid photothermal CVD,[10] remote plasma enhanced (RPE) CVD, and jet vapor deposition based CVD are also being investigated.

Recently, Ma and co-workers[11] have used a cluster tool to deposit ultrathin oxide/nitride stacked layers. The in-situ process consist of the following four steps: (a) growth of 0.5-0.6 nm oxide by plasma oxidation, (b) deposition of oxide by RPECVD, (c) deposition of nitride by RPECVD, and (d) post-deposition rapid thermal annealing at 900°C for 15 seconds in nitrogen gas. The equivalent oxide thickness was 2.5 nm, and poly-Si was used as the gate. For comparison purposes, a thermal oxide was also grown. Current-voltage measurements of the stacked dielectric showed that there are no trapped charges at the oxide/nitride interface. However, as compared to the thermal oxide, the oxide/nitride stacked dielectric showed degradation in channel mobility and lower drive current.[11]

In a recent publication,[12] in-situ RTCVD has been used to grow a passivation layer of 0.6-0.7 nm in NO at 800°C. Si_3N_4 films were deposited at 800°C followed by rapid thermal annealing (RTA) at various temperatures. For equivalent oxide thickness, comparable or better results were claimed for the stacked dielectric.[12] However, for a gate-voltage of about 1 V there was no difference in the transistor characteristics of the thermal oxide and stacked gate dielectric.

Ultra high vacuum CVD has been used to deposit tungsten films at a temperature of ~ 450-600°C on top of 3 nm thermal oxide.[13] The current density-voltage characteristics of the tungsten gate are comparable to a poly-Si gate. The tungsten-SiO_2-Si capacitor could also withstand RTA at 950°C for 5 seconds.

Researchers at Bell Laboratories have used in-situ cleaning of HF gas followed by ultra violet (UV) cleaning before rapid thermal oxidation. Such ultrathin (< 2 nm) oxides have shown very low gate leakage current.[14] The highest transconductance that has ever been reported for any Si transistor uses ultrathin oxides formed by RTP. Details of the ultrathin oxide work may be found in Ref. 7.

In a recent publication, it has been shown that using UV and ozone, good quality thin (1-2.5 nm) oxides can be grown at very low temperature (25-600°C).[15] Oxides grown by this method appear to be comparable in electrical quality to thermal oxides. The degradation of ultrathin gate oxides during plasma processing is also a matter of concern. Plasma induced gate oxide damage depends on equipment type, etching gas, and/or etching conditions. Adding an insulator to the back of the wafer can reduce charging. An in-line damage measurement technique can rapidly detect and solve gate oxide damage problems in a manufacturing facility.[16]

Defects and Reliability Issues

A number of processing techniques have been used to grow or deposit ultrathin dielectrics. Recent work[17] has shown the existence of a dense (~2.4 gm/cm^3) thin (~1 nm) layer at the SiO_2/Si(100) interface. The density of oxide at the interface is higher than the bulk density of SiO_2 or Si. The extent of bulk built in-strain can be detected by an infrared absorption band due to the longitudinal optical (LO) phonon mode operating from the Si-O-Si lattice vibration. As shown in Fig. 3, a distinct red shift of the LO phonon peak is observed within 2 nm from the interface.[17]

From a reliability point of view, trap generation is important for ultrathin dielectrics. A recent tutorial has reviewed oxide wearout, breakdown, and reliability of gate oxides.[18] The wearout process has the same field, time, and temperature dependence, as does dielectric breakdown. The wearout can be described in terms of trap generation, probably involving the rupture of strained Si—O bonds in a $_3O{\equiv}Si—O—Si{\equiv}O_3$ moiety as shown in Fig. 4.[18] The O atom in the bridge may then drift away, leaving a classic E' center, with a positive charge on one Si, and a dangling orbital on the other. Such a defect center can trap an additional electron, and then detrap it. Further details of physical trap generation are described in Ref. 19. Both the number of bonds and the bond energy distribution vary with the bond angle. The weakest bonds (those close to 120° and 180°) would be the first bonds broken by the field. The understanding of trap generation and related kinetics is very important for using Si based ultrathin dielectrics. In essence, atomic (nanoscale)-roughness at the Si-SiO_2 interface and structural inhomogeneity are largely responsible for the reliability problem in silicon-based ultrathin dielectrics.

Process Integration and Manufacturability

Silicon-based ultrathin dielectrics will be used mostly in the manufacturing of sub-100 nm CMOS transistors (fabricated on 12 inch or larger diameter wafers) operating mostly at 1 V or lower voltages. Reduction of defects has been very important all along the growth of the silicon IC industry. However, for sub-100 nm technologies, defect detection and defect reduction will become the most important manufacturing criterion. The results presented in this paper show that there are a number of directions that are currently being explored for processing of ultrathin dielectrics. The use of 12 inch and larger diameter wafers will force the manufacturers to reduce the processing temperatures to about 900°C or below. It is well known that at lower processing temperature the quality of dielectrics is inferior compared to dielectrics processed at higher processing temperatures. Thus at a lower processing temperature, additional activation energy for a thermal process can be provided by using plasmas, photons, ions, or by a supersonic jet. Out of all these additional sources of energy, the use of UV and vacuum ultra violet (VUV) photons for in-situ substrate cleaning, growth or deposition, and in-situ annealing is very attractive, since these photons can provide beneficial effects in reducing microscopic defects, processing temperature, and processing time.

Rapid thermal processing has the advantage that substrate temperature can act as a chemical switch. This type of dual spectral source rapid photothermal processing (RPP) can reduce the atomic roughness of the processed dielectrics.[20] This is due to the fact that in any deposition or growth process, one of the main reasons for the formation of surface roughness and defects is because of the statistical fluctuations in the arrival rate of the vapor flux. This fluctuation in the flux increases with an increase in the processing temperature. During deposition, statistical roughening and surface diffusion compete with

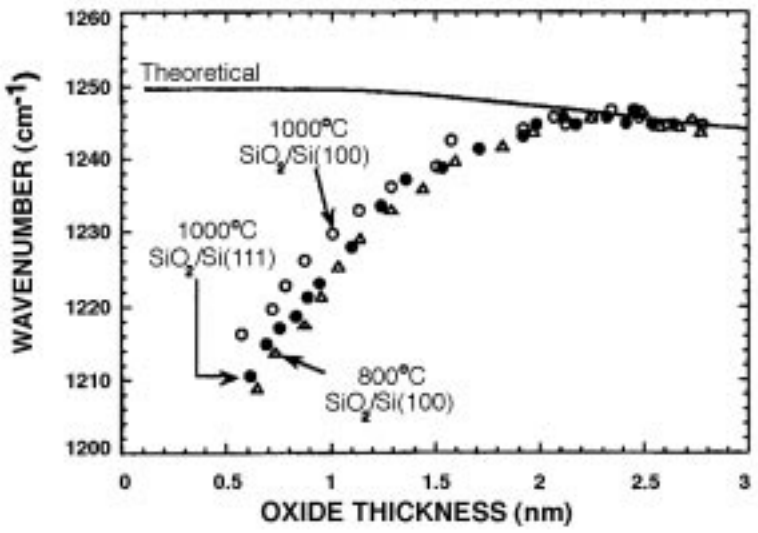

FIG. 3. The absorption peak wavenumber due to the LO phonon mode as a function of oxide thickness for ~2.8 nm thick dry oxides grown on Si(100) or Si(111). The solid line indicates the calculated LO phonon peak wavenumber versus oxide thickness for well relaxed bulk SiO_2 (from Ref. 17).

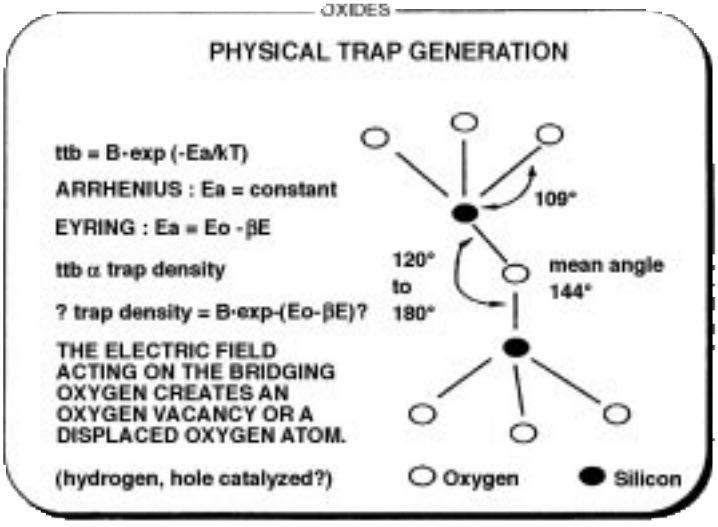

Fig. 4. Schematic diagram showing that the bridging oxygen bond is responsible for physical trap generation (Figure courtesy of D. Dumin, see Ref. 18.)

each other, the first increasing the film roughness and the second smoothing it out. The use of UV and VUV photons in any thermal process provides higher bulk and surface diffusion coefficients.[20] As a result, RPP provides a lower temperature for the process, reducing statistical fluctuations and also increasing the surface migration, thus reducing surface and interface roughness.

Conclusion

In this paper we have examined the current status of silicon based ultrathin dielectrics. Minimization of atomic (nanoscale) roughness at the interface of Si and silicon dioxide is very important for obtaining high quality dielectric films. Processing techniques that can reduce processing temperature and provide a homogenous microstructure resulting in an atomically smooth conductor (poly-Si or metal)/dielectric interface will be used in the manufacturing of reliable circuits. No single processing technique has emerged as a clear-cut winner. Fundamental understanding of the origin of defects is most important for the manufacturing of silicon CMOS circuits based on ultrathin dielectrics.

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