450 mm Silicon: An Opportunity and Wafer Scaling

by Masaharu Watanabe and Scott Kramer

oday, we take our favorite music and movies anywhere. It is a result of the never-ending reduction in bit cost brought about by the accelerating development of semiconductor devices and their production technology. The wellknown Moore's law is a core of the International Technology Roadmap of Semiconductors (ITRS)¹ that serves as a technology target for the semiconductor industry. An increase in silicon wafer size is embedded in it for more efficient and economical production of devices. Silicon as a key material² of the electronics industry undergoes progress in defect engineering and production technology. The ITRS indicates that the next generation wafer size, of 450 mm, will be in production in 2012. In the 450 mm era, silicon wafer suppliers will grow a larger and consequently heavier single crystal ingot than ever before, 215 cm long and weighing 800 kg.3 At the beginning of the 300 mm era, there were intense discussions⁴ related to inexperienced 300 mm crystal and wafer technology. These discussions also provided useful information beyond the 300 mm technology. Super Silicon Crystal Research Initiative Corp. (SSi) pioneered the growth of a 400 mm crystal.5 How the 450 mm crystal will come to production, and whether it is economically feasible, is now a hot topic in the silicon industry.^{6,7} The first 450 mm wafer was displayed at SEMICON West in 2006, which sparked industrial interest. This article presents a brief description of emerging 450 mm wafer technology issues.

In the last 300 mm transition, the industry, for the first time, held global discussions to synchronize efforts to reduce cost and facilitate a smooth transition. For the coming 450 mm transition, more collaboration and deep discussion on the transition scenario will be indispensable.

Lessons Learned from 300 mm

The 300 mm transition clearly exposed the need for industry collaboration in all aspects of a transition to the next wafer size. Each wafer size transition becomes more challenging as complexity increases, business models diverge, technology advances, and economic and market dynamics come into play. For the next wafer size transition, it will be particularly important for the factory architecture to be adaptable across all business models in IC manufacturing: DRAM, high volume microprocessors, foundry, and very high mix logic. Based on historical production wafer development cycles, research and collaboration must start early enough for the industry to achieve consensus on a wafer strategy to ensure availability of supply when needed. Industry dialogue, data collection, and analysis of timing, risk, and time to ROI, as well as technical challenges and initial wafer, have been initiated. This dialog will provide the information needed to continuously evaluate and adjust plans across the industry. In addition, economic analysis and factory simulation are even more important. Fortunately, in the years since the 300 mm transition, modeling software has increased dramatically in terms of function and speed. That software has the capability to model very complex interactions in a short period of time.

Economics of 450 mm Wafers

The economic situation is the most important concern in the semiconductor industry. Moore's law, in the form of "more function by same cost," drives our technology. One scenario to reduce bit cost, by employing the next generation large diameter wafer, is that wafer and device production equipment prices do not increase as wafer area increases; and production throughput does not significantly decrease while keeping the same device yield. It worked well in the 300 mm transition; but when and what device production will be converted from 300 mm to 450 mm, and the investment needed, are not yet clear.

The production of 450 mm wafers is economics driven and fab cost is the largest economic factor. Single crystal cost depends on crystal growth conditions such as the slower growth rate of a 450 mm crystal, compared to current 300 mm crystal growth, and lower poly silicon usage. Wafer cost depends on wafer shaping, especially wafer thickness that increases for the larger diameter. These are inevitable factors that push up wafer cost/area.

Historically, silicon suppliers have developed new growth technologies to meet industry demand and to maintain competitiveness. However, the 450 mm case will be different. The expected R&D cost to develop a 450 mm wafer pilot production fab will be so large that some silicon suppliers will hesitate to start 450 mm R&D. Recent poly silicon shortage by strong solar cell demand and the resulting increase in price9 will certainly push up the R&D cost. Cooperation among industry and research institutes, or any kind of joint work in the pre-competitive area, will help to reduce the industry's R&D cost. Some discussions are already occurring in the industry.6

Technical Opportunities

450 mm crystal growth.—450 mm crystals are estimated to be so big (215 cm) and heavy (800 kg) that their growth will have many challenging issues,³ as shown in Fig. 1. The SSi project was pioneering work, making the issues clear and showing the feasibility of a 400 mm crystal.5 Learning involves a so-called Dash neck growth that will be discussed in detail in the following section. The other is the design of a crystal puller and growth process. Practical simulation is inevitable to develop 450 mm crystal technology since experimental works are quite limited due to a weeklong growth cycle and high cost. Sophisticated experimental design, based on intensive simulation, will be extremely useful and is really key for the 450 mm R&D. For point defects, such as vacancies and interstitials, their control is a most competitive part of crystal growth technology. The expected narrowing of choice of growth conditions¹⁰ to balance vacancies and interstitials in the 450 mm crystal growth will be overcome by the improved thermal design crystal puller.11 Published data of SSi's 400 mm crystal12 show that both vacancy rich and interstitial rich crystals could be grown by a choice of growth rate. This encourages 450 mm crystal engineers to optimize hot zone (crucible, heater, heat shield, etc.) design and growth rate.

Neck issues.—All silicon crystals for LSI are dislocation-free, that is, the whole of the grown crystal ingot of a few 100 kg weight is completely free of dislocations. At the beginning, the Dash neck, which is a few millimeter in diameter thin single crystal, is grown to eliminate dislocations. The whole of the crystal is sustained by the Dash neck, no matter how large



FIG. 1. 450 mm silicon single crystal growth issue. Poly silicon (1000 kg) is melted in quartz crucible and a Dash neck of several mm is grown to start dislocation-free crystal growth. Growth of a more than 900 kg crystal will take 3-5 days. A new mechanism is required to sustain such a heavy crystal. About 800 kg can be used for wafer production.

and heavy the ingot finally comes. Dash neck strength is roughly 144 kg/3 mm-diameter-neck.¹³ In the 450 mm case, and even the 400 mm case of SSi, the neck is not expected to be able to sustain a heavy crystal. Thus, some breakthrough was required. SSi developed a two-step growth technique.¹² A Dash neck was first grown to eliminate dislocations. Then a second suspending cone was grown to support the heavy crystal weight by the other mechanics. A special tool, called a clamp or tray, held the cone and sustained the weight of the crystal body afterward. The strength

of 3 mm neck is not enough even for the current 300 mm crystals. An alternative to the two-step growth is a thick Dash neck. Industry grows current dislocation-free crystals with a thicker neck. Developing a thicker (~9 mm) neck is, though it is not easy, a possible alternative solution for the 450 mm crystal.

450 mm wafer shaping.—Wafer shaping is an extension of the current technology. Wafer specification, like flatness, links to lithography technology and becomes tighter and tighter. So, both large diameter and tight control, as shown in Fig. 2,



FIG. 2. 450 mm polished wafer issue. The issue of the 450 mm wafer is its thickness. When the wafer is supported at its periphery, sag due to weight is large. Wafer flatness near the edge is a difficult challenge. Edge shape and damage should be considered carefully to avoid wafer breakage.

impose intense work for the production of 450 mm wafers. Wafer shape near the edge, especially flatness, will be a key issue.

Scaling

Along with Moore's law, many scaling factors are compiled in ITRS. The current wafer diameter trend is 450 mm production for 2012 and beyond. A wafer property that is particular to the wafer diameter is the wafer thickness. Thickness and others factors related to 450 mm are considered here from the scaling point of view.⁶

Crystal Growth Scaling

Major silicon suppliers participated in the SSi project, which pointed out issues associated with a large crystal growth. Based on their experience, thermal and mechanical design of a crystal puller can be scaled up from the current 300 mm puller to a 450 mm puller, using the latest simulator running on a powerful computer. Many things still need to be solved to start real production. SSi grew a 400 mm crystal at the rate of 0.45 and 0.25mm/min.12 A 450 mm crystal will take 5 to 8 days to grow, including poly silicon melting, growing the crystal, cooling, and preparing the puller for the next growth.

Wafer Thickness Scaling

Wafer thickness should be considered carefully. Once it is decided, it is difficult to change afterwards. Many device production technologies and much equipment are wafer thickness dependent and a change of wafer thickness has a major impact. Thickness factors to be taken into consideration include: empirical extrapolation without clear reason; slip generation due to thermal stress; sag due to wafer weight and any elastic deformation due to film stress; and wafer breakage due to wafer handling, thermal stress, and others.

Empirical scaling.—Historically, wafer thickness has been increased by some factor as the wafer diameter steps up to the next diameter, because thin large wafers may be fragile and hard to handle. As shown in Fig. 3, extrapolation of the rather recent 125 mm, 200 mm, and 300 mm diameters trend to 450 mm indicates that 450 mm wafer thickness would be about 825 $\mu m.$ Third order polynomial curve fitting to semilog plot of diameter trends indicate that the 450 mm wafer thickness would be about $800\ \mu m.$ This is a simple empirical extension of the historical diameter trend and 25 μm to 50 μm thicker

than current 775 μm thick 300 mm wafer. SSi estimated 825 μm for 400 mm and 875 μm for 450 mm. 5

Scaling based on thermal stress.-Thermal stress can be, in general, thickness sensitive in two aspects. One is a slip generation by plastic deformation due to shear stress at high temperature processes. The other is wafer breakage caused by the tensile stress, also at high temperature processes. A flash lamp annealing (FLA) process to activate ion implanted impurities is the most high temperature single wafer process that is 1200°C or higher for a few mseconds in current 300 mm processes and is expected to be the most severe process in the 450 mm era. Stress analysis shows that shear stress in 450 mm wafers due to the FLA has almost no wafer thickness dependence. Tensile stress is also almost thickness independent, about 10% larger than 300 mm wafer. Thermal stress at vertical diffusion furnace processes such as oxidation will be more sensitive to wafer diameters because the wafers are stacked with critical spacing. However, the thermal stress difference is less than 5%. So, the thermal stress issue of both single and batch wafer processes does not depend so much on wafer diameter or thickness and will not be a crucial scaling factor.

Scaling based on sag.—Sag is due to wafer weight and also due to strain caused intentionally or by films on the surface. Sag is an important factor in wafer handling. Gravity sag, that is, sag by wafer weight, is a classical plate bending. Sag (δ) of circular plate support at the wafer periphery is proportional to

$$\begin{split} \delta &= k R^4 / D \\ D &= E t^3 / 12 (1 - \nu) \end{split}$$

where R is wafer radius, E is Young's modulus, v is Poisson ratio, t is thickness, scaling factor is R^4/t^3 . Sag of 775 µm thick 450 mm wafer supported by 4 points at wafer periphery is 687 µm. If sag needs to be the same as 300 mm, that is 136 µm, the 450 mm wafer should be 1744 µm thick. A wafer of this thickness is heavy and will definitely be expensive. It is not a practical choice.

Sag due to film on the wafer surface is

 $\delta = 6R^2(1-\nu)\sigma/(Et^2)$

where σ is film stress and the scaling factor is R²/t². So, if the film stress is same, the sag of a 775 μ m thick 450 mm wafer is 2.25 times 300 mm wafer. If the above sag is acceptable by proper design of wafer handling system and process conditions, a 450 mm wafer of the same thickness as a 300 mm wafer can be used.



FIG. 3. Wafer thickness scaling. Thickness trend of SEMI wafer specification is plotted in semilog scale. Linear and 3rd order polynomial fits are shown. Extrapolating this empirical scaling to 450 mm, thickness is 800 μ m to 825 μ m. First proposal is 825 μ m, that is 775 μ m and additional 50 μ m for reclaim.

Scaling based on wafer strength.-Thinner wafers are often supposed to be more fragile. Wafer breakage is complicated and probability is very low. Scaling of wafer thickness based on the breakage is important but model is hardly available. Bare wafer breakage is reported occasionally.¹⁴⁻¹⁶ Some wafers break during VLSI fabrication processes influenced by oxygen precipitates.¹⁷ The edge polish process introduces some damage.¹⁸ If it causes wafer breakage, the 1.5 times longer edge of a 450 mm wafer compared to a 300 mm wafer will result in more chance of breakage, according to Weibull statistics. A wafer vibrates during handling.19 If the breakage is caused by wafer handling or any process touching wafer, it will depend on the wafer thickness, wafer weight, back surface and edge area, and edge shape. Again, no model based on solid mechanics or statistics is available. A different approach to the fracture issue is the increase of the fracture strength by nitrogen doped Czochralski crystal.20

Mechanical Wafers

In the ITRS,¹ wafer standards need to be discussed first because wafer geometry, especially thickness, influences equipment design. Wafers that are used for equipment development are called mechanical wafers. If reclaim of wafers by repolishing of surface layer is considered, another 50 µm needs to be added to thickness as a buffer. Then, 825 µm (the current 300 mm thickness plus 50 μ m) is a first assumption of 450 mm wafer thickness. Other wafer geometry properties like notch, edge shape, and surface finish are the same as a 300 mm wafer.

Summary

In the ITRS, device production using 450 mm wafers is projected to start in 2012. The SSi project showed the feasibility of 400 mm wafer technology. Discussions on 450 mm issues have been ongoing in the last few years. Crystal growth of 450 mm is technically possible although many issues must be solved to prepare for real production. Empirical extension of wafer thickness trend to 450 mm indicates 800 µm to 825 µm. Wafer thickness has been discussed here from various scaling perspectives but none is crucial so far. The first proposal is 825 µm that is 775 µm (current 300 mm wafer thickness plus 50 µm for reclaim). The economics of 450 mm wafer production is the most important issue currently under discussion and when and how the 450 mm era actually comes is not vet clear. The lessons learned from the 300 mm wafer technology will help immensely in the coming 450 mm transition.

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