Advanced Electronic Substrates for the Nanotechnology Era

by Carlos Mazuré and George K. Celler

For the last few decades the performance of silicon integrated circuits has steadily progressed, as anticipated by Moore's law, primarily through scaling of all critical device dimensions.[1] This classical scaling is either no longer possible (for example gate SiO_2 thickness has reached its limit) or does not allow achieving the targeted device performance increase per technology node. Starting with the 90 nm technology, innovations other than simple scaling are the main contributors to better performance.

Substrate engineering[2,3] has enabled the industry to overcome many of the limitations encountered by traditional scaling. As a result, device architecture and engineered substrates have become strongly coupled, a coupling that is growing stronger as the IC industry moves to the 65 nm technology node and beyond. Substrate engineering started in earnest with the industry transition to SOI wafers in the late '90s.[4-7] SOI substrates made possible increasing the drive current while simultaneously reducing parasitic leakage, thus improving IC performance and reducing power consumption. SOI has allowed the IC industry to develop superb solutions for high performance logic, including the latest gaming-dedicated microprocessors.[8-10] Other highly competitive designs address "smart power" for automotive,[11] and very low power ICs for consumer applications.[12] In more recent advances beyond conventional SOI, new substrates like strained SOI[13-17] and hybrid bonding SOI[18-20] have increased the number of options for enhancing device mobility.

While the 90 nm node is characterized by the adoption of SOI for high performance applications,[8-10] the future nodes are driving numerous substrate solutions. The device development of the future technology nodes appears to be marked by two distinct technical strategies, one focused on high performance, and one driven by system-on-chip (SOC) applications, including low power, portable RF applications. Figure 1 is a tentative device roadmap for logic applications. Today's partially depleted (PD) transistor architecture may evolve into a fully depleted (FD) approach. High performance logic utilizes uniaxial tensile strain for n channels and compressive strain for p channels in order to boost carrier mobility. Wafer level tensile biaxial strain will further enhance the channel engineering possibilities. Three-dimensional devices like FinFETs[21,22] may supplement and eventually replace planar device structures.[1] SOC applications will push PD SOI and high impedance SOI designs, possibly transitioning over to FD designs for very low power applications. Figure 1 is also a good illustration of some of the engineered substrate options being evaluated for the 65, 45, and 32 nm nodes.

The high performance path will continue to be the driver for the most advanced substrates and the material innovation. Ultra-thin (UT) SOI, mobility enhancing substrates like strained SOI (sSOI), in addition to local strain techniques, as well as improved thermal dissipation to reduce the impact of hot spots on MOSFET performance, are among the most obvious engineered substrate solutions. Device architectures are likely to remain planar at least for the next two generations, with non-planar FinFETs on the horizon for the 32 nm node for the most aggressive IC players. Partially depleted approaches will push the mobility enhancing substrates while others may switch to ultra-thin fully depleted SOI in order to improve electrostatic device characteristics. Each way presents its own set of technical advantages and challenges.

For advanced RF SOCs, high impedance SOI substrates with a high resistivity handle wafer provide significant advantages,[23] while SOI with ultra thin buried oxide (<50 nm) will enable IC architectures where n and p regions are defined in the handle substrate for back bias generation through the buried oxide.[24] Since attaining the highest performance is not the focus here, these SOI CMOS solutions will target the lowest power consumption and longest battery lifetime. Low standby and low operating power devices will be built by taking full advantage of dielectric isolation, while high resistivity substrates will substantially improve performance of passive components such as inductors that are placed directly on the silicon chip.

SOI Substrate Fabrication

Silicon on Insulator (SOI) technology was initiated in the 1960s by the demands of radiation-hard circuits. During 1970s and '80s several SOI materials and structures were conceived for dielectrically separating the thin, active device volume from the silicon substrate.[5-7] The background idea is that in a bulk silicon MOS transistor, only a superficial layer, typically <100 nm thick, is actually useful for electron transport, whereas the substrate causes undesirable effects.

The overwhelming success of bulk-Si CMOS confined SOI technology to niche applications until late 1990s. Then several factors have increased the interest in SOI: invention of new fabrication methods for SOI

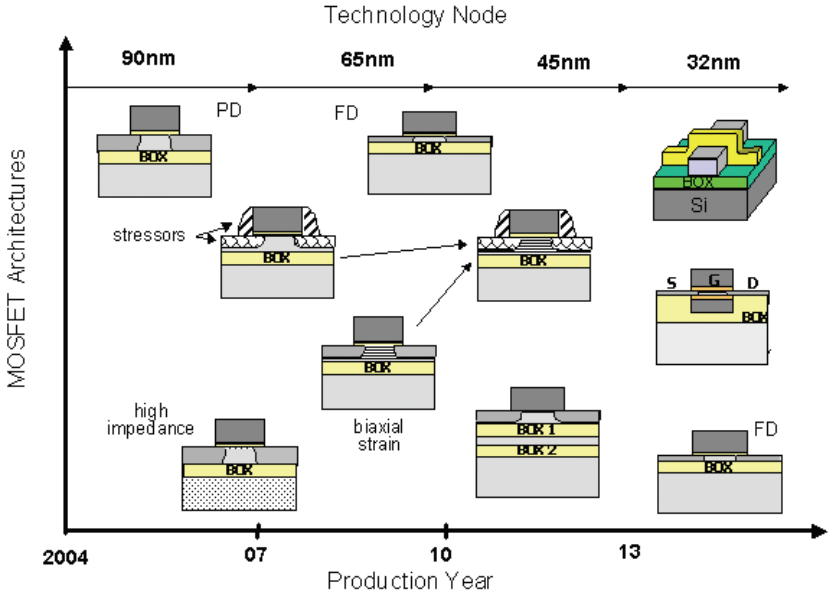

Fig. 1. *Device architectures that are either already in use or are anticipated in future technology nodes.*

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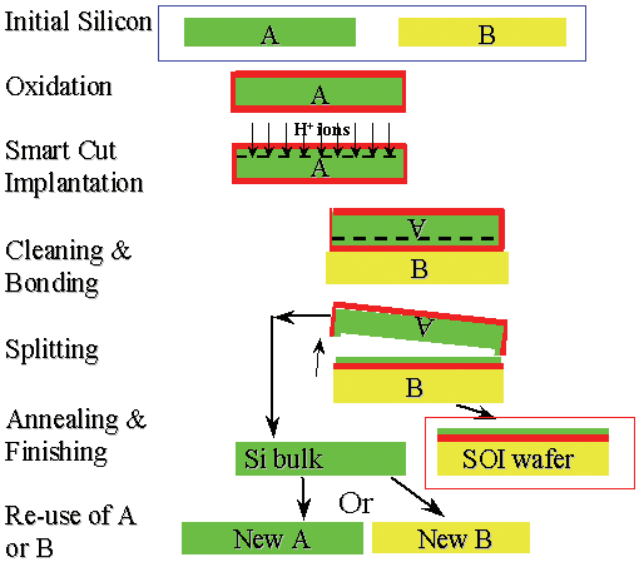

FIG. 2. A schematic process flow for SOI wafer fabrication by Smart Cut™ technology.

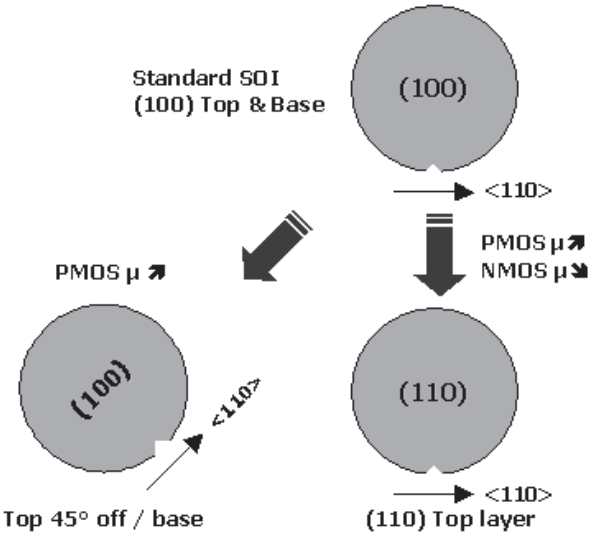

FIG. 3. Crystalline plane orientations and directions within the planes that improve electron and/or hole mobility in Si MOSFETs.

materials and their optimization, need for lower power and higher speed circuits, emerging limitations of bulk CMOS scaling. SOI transistors are now unchallenged in extending the frontiers of ultimate CMOS scaling.

Epitaxy and single crystal layer transfer are the two most critical processes for substrate engineering that allow the tailoring of the composite substrate to the application. Smart Cut™ technology is the dominant method for thin layer transfer and SOI fabrication.[25-27] It consists in defining a splitting region within the donor substrate by ion implantation (*e.g.* H^+ or He^+) that allows transferring a thin film to a handle wafer by means of bonding followed by splitting. The first industrial implementation of the Smart Cut technology is SOI manufacturing. The simplicity of the concept is schematically illustrated in Fig. 2. First, a thermal oxide is formed on the donor wafer followed by hydrogen implantation with doses typically in the mid $10^{16}cm^{-2}$ range. The implantation energy determines the thickness of the transferred layer; the thermal oxide thickness defines thickness of the buried oxide (BOX) in the final SOI structure. After cleaning and surface activation, the donor and handle wafers are bonded together. By splitting at the H^+ implanted region, a thin film is transferred to the handle substrate. Subsequent steps remove the post-splitting surface roughness. Since the thickness removed from the donor wafer is negligible compared to the total wafer thickness, the donor wafer can be reused many times. A range of thicknesses from 10 nm up to a few 10^3 nm for both top Si and BOX films is easily covered by this technology with standard industrial implanters and furnaces.

The Smart Cut technology is a powerful tool that applies to many materials, making it possible to create a wide range of composite substrates and their tailoring to the requirements of the application by properly choosing the active layer, the buried dielectric and the base substrate.[28,29]

High Resistivity SOI

Cross-talk between RF analog circuits and digital logic contained within the same "mixed signal" chips is reduced in SOI substrates. High impedance SOI, *i.e.* SOI in which the handle substrate has resistivity >1 kOhm-cm, enhances these advantages and improves performance of monolithically integrated passive components, such as inductors.

SOI technology provides complete oxide isolation, cutting off direct paths of substrate injection noise and a high resistivity substrate reduces the capacitive coupling, thus further reducing the substrate related RF loss. Because of the SOI-inherent isolation of the high impedance substrate, device latchup is not an issue.

Patterned ground shields (PGS) are used in Si bulk wafers to manufacture high quality factor Q inductors. In SOI these can be avoided and better Q factors are achieved even at higher frequencies. Typically 50% greater Q is achieved with high resistivity SOI (SOI HR) as compared to bulk.[23] Coplanar transmission line measurements on SOI HR show that a loss better than 0.5 dB/mm at 40 GHz and 1 dB/mm at 80 GHz can be achieved. At these values integrated passive components in SOI HR become comparable to what can be achieved on InP.

Substrates with Enhanced Charge Carrier Mobility

Mobility enhancing substrates are emerging as an essential tool in the effort to continue improving Si circuit performance by 17% per year, as dictated by the ITRS.[1] Two major approaches are hybrid orientation SOI and strained silicon SOI. In the first case, a composite substrate is built with (110) and (100) crystal orientation regions for the p- and n-channels, respectively.[20] In the second case, a biaxially strained Si film is used as the top SOI layer to boost the electron mobility.[13-17]

Mobility optimization in composite wafers with hybrid crystal orientation (SOI and DSB).—Traditional (100) Si substrate orientation serves well NMOS transistors as electron mobility is near its peak in such a configuration. However hole mobility in the (110) plane is approximately double of that for the (100) surface plane. Substrate engineering permits optimizing NMOS and PMOS performance simultaneously by means of using composite substrates that contain both crystal orientations. Hybrid orientation composite SOI is fabricated by transferring a (110) Si layer onto a (100) handle wafer as schematically shown in Fig. 3. Another variation is a (100) film on a (110) substrate.

For 40 nm long p-MOSFETs fabricated on a (110) surface a current drive increase of 45% is achieved, but in contrast, the n-MOSFET on the (110) plane is degraded by 35%.[20,30] To overcome this problem, windows corresponding to the n channel regions are etched in the substrate through the buried oxide down to the (100) handle substrate. Then Si

selective epitaxial growth follows after a spacer formation. A strong overgrowth is required to drive defects out of the active area with facet formation above the substrate plane. A final CMP step planarizes the topography and a composite wafer with (110) and (100) regions embedded in the same surface are obtained.[20] The obvious drawback of this approach is that one of the devices is fabricated on bulk.

Although SOI structures provide many advantages, circuits that are specifically designed for bulk silicon can also utilize hybrid orientation substrates. In such cases the composite wafers also contain two crystal orientations as described above, but the intervening buried oxide (BOX) is eliminated as shown in TEM cross sections of Fig. 4.[31] Such wafers, known as DSB for Direct Silicon Bonding, are another example of enhancements that are possible because of layer transfer. In order to access both orientations at the wafer surface, the same approach as for hybrid SOI wafers can be taken. However, a simpler and potentially more cost-effective method of selective amorphization and templated re-gr owth has been described recently.[32,33]

Some enhancement in CMOS performance can be obtained by a less complex but also less effective PMOS mobility enhancing substrate that is obtained simply by rotating the top (100) Si film with respect to the (100) substrate by 45°.[18,19]

Strained SOI (sSOI).—A powerful technique for increasing carrier mobility and current drive in CMOS involves introducing strain into transistor channels. Uniaxial local strain—obtained, for example, by using recessed SiGe stressors in p-MOSFETs[34] or compressive and tensile nitride encapsulation for p- and n-channels, respectively,[35] is presently a well established technology. Another approach that we will describe here is based on biaxial tensile wafer-level strain. The biaxial tensile strain lifts the conduction band degeneracy between the in-plane and the out-of-plane valleys, and as a consequence it enhances carrier mobility by means of reduced intervalley scattering and a smaller in-plane electron effective mass.[36] A similar effect is achieved for holes for significantly higher levels of strain that lifts the heavy and light hole degeneracy.

The final mobility and current drive increase of n- and p-channel devices depend on the Ge content of the SiGe template used to create the strain.[16,37] For a strained Si film grown on a fully relaxed SiGe (20% Ge) template, a biaxial stress level of 1.3 GPa is achieved.[13,17,38] This leads to a mobility enhancement of 80%

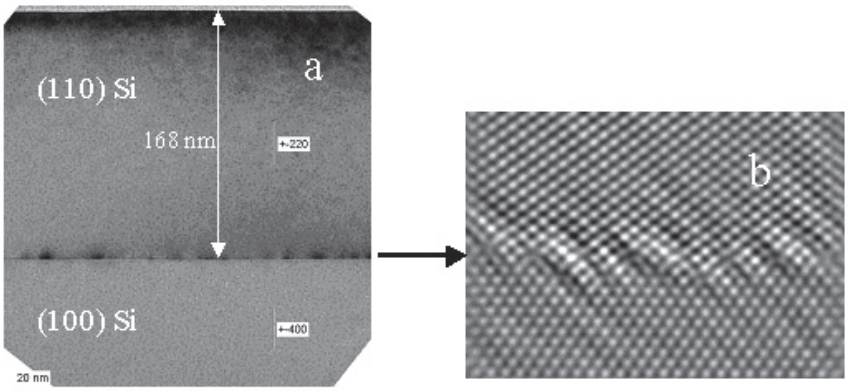

Fig. 4. *(a) XTEM image of the DSB wafer and (b) XRTEM image of the bonding interface (from Ref. 31).*

for the n-MOSFETs, resulting in an increase of 40% in the current drive. If the concentration of Ge is increased up to 40%, the same level of mobility enhancement is also achieved for p-channels.[16,39,40] Currently, substrates originating from 20%Ge template, with strained silicon directly on insulator (sSOI) are commercially available and are being evaluated by the IC industry.

Fabrication of sSOI[13] has many steps in common with the SOI process flow shown in Fig. 2. Device processing in sSOI substrates can be done with

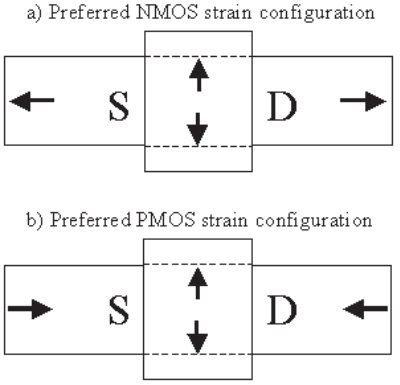

Fig. 5. *Ideal strain configurations for n-MOS and p-MOS transistors (after Ref. 42).*

conventional thermal budgets, as there is no strain relaxation up to 1100°C if proper surface passivation is applied. Typical strained Si film thickness varies from 10-20 nm for FD devices architectures and up to 70 nm for full compatibility with existing PD designs. Typical stress values are 1.3 GPa ±20 MPa, one sigma variation.[17]

The scalability of sSOI has been thoroughly investigated for ultrathin body sSOI[14,15] with the fabrication of short channel devices. More recently, the impact of 40 to 50 nm thick sSOI on PD MOSFETs has been reported,[41] showing a 30% reduction in gate oxide leakage and a 60% improvement of the SRAM write margins. An important result of this work is that it shows that even for super-critical thicknesses the strained Si film does not relax after patterning and device fabrication if appropriate care is given. The strain in the active areas is monitored electrically through a threshold voltage V_T shift that is a result of the smaller band gap of the strained Si film. The threading dislocations defectivity of sSOI has been improved to $<10^4$ cm^{-2}.

For moderately strained Si, such as obtained by Si epitaxy on 20% Ge SiGe, the dilemma is that simple biaxial tensile strain is beneficial for n-MOSFETs but somewhat detrimental for p-MOSFETs. To fully exploit the potential of sSOI substrates, strain hybridization is essential. Figure 5 shows the preferred strain configurations for n-MOS and p-MOS. In an n-NMOS device (Fig. 5a), biaxial tensile strain as provided in sSOI is shown. This enhances current drive. Any additional process-induced uniaxial tensile strain can be superimposed on the substrate level strain for even greater performance boost. This is demonstrated in data from Thean *et al.*[42] in Fig. 6, where adding uniaxial strain to conventional SOI increases the drive current by 9% but adding the same tensile etch stop (tESL) layer to sSOI gives a total boost of 9%+18% as compared to SOI alone. In other words, everything else being equal, sSOI improves the current by 18%.

Figure 5b shows the ideal strain configuration for p-MOS as determined from piezoelectric coefficients of silicon—uniaxial compression along the current flow and tension in the direction normal to it. This configuration cannot be obtained by either substrate level or process-induced strain alone. Compression along the current flow axis can be produced by strained nitride etch stop layers and/or by SiGe epitaxial layers embedded in the source/drain regions. STI (shallow

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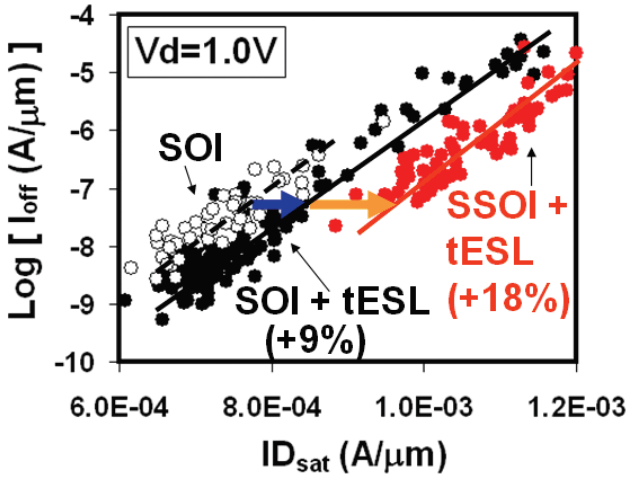

FIG. 6. Drive current ID_{sat} vs. I_{off} for n-MOS devices with various stressors (from Ref. 42).

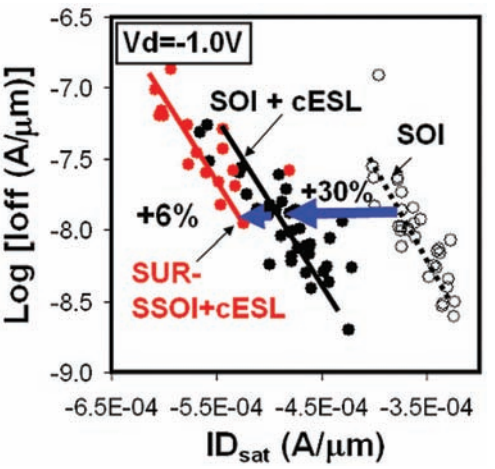

FIG. 7. Drive current ID_{sat} vs. I_{off} for p-MOS devices with various stressors (from Ref. 42).

trench isolation) can produce compression along one or both lateral axes, depending on device geometry.

However, to obtain the desired configuration as shown in Fig. 5b, it is necessary to combine an sSOI substrate with process-induced strain, for example with cESL. For best results, during device processing on sSOI an additional step of Selective Uniaxial Relaxation (SUR) is implemented to eliminate tensile strain parallel to the device axis, while preserving the transverse tensile strain. Subsequently, conventional uniaxial compressive stressors are applied. The finished p-MOS devices have the most desired configuration (Fig. 5b) with uniaxial tension perpendicular to the current and uniaxial compression along the current. Data in Fig. 7 show that cESL alone improves ID_{sat} by 30%, but sSOI with SUR adds another 6%. Further optimization is expected to yield much greater enhancements.

To summarize, by combining uniaxial stressors with a biaxially tensile starting sSOI substrate, both n-MOS and p-MOS devices are improved beyond what would be possible with process-induced strain alone.

Band-gap engineering - dual channel MOSFETs.—The combination of epitaxy and layer transfer opens up a multitude of possibilities to modify the band structure and take the mobility enhancement beyond the present sSOI.[43,44] Dual channel is an example of a band structure engineered by epitaxy. Figure 8 shows the results for a composite top layer of strained Si/strained $Si_{0.4}Ge_{0.6}$/relaxed $Si_{0.7}Ge_{0.3}$. A hole mobility increase by a factor of 2-3 can be obtained, even at high carrier densities, as compared to SOI or SGOI substrates.[43]

Germanium on Insulator (GeOI)

GeOI[45-47] is the newest development among the mobility enhancing substrates. It is of interest for high performance CMOS ICs[48] as well as for photodetectors and solar cells.[49] The Ge donor wafer can be an epitaxially grown Ge layer on a Si substrate or a Ge bulk wafer. Ge bulk wafers are heavier than Si and brittle. GeOI helps overcome these issues and makes Ge MOSFET technology compatible with Si processing facilities. The epitaxial approach to the Ge donor is easily scalable to 300 mm but suffers from high crystal defectivity. Processing a Ge surface is a difficult task because the typical Si cleaning solutions etch and roughen the Ge surface. Although GeOI processing in a Si facility and the fabrication of 0.15 μm devices has been demonstrated,[50] MOSFET I_{on}/I_{off} ratios are poor and mobility values need to be improved. MOSFET quality on Ge surfaces is an issue that needs to be addressed for Ge and GeOI substrates alike. The main question that will have to be addressed as GeOI technology progresses is the impact of the narrow band gap of Ge (0.66 eV) on junction leakage and band-to-band tunneling.

SOI with Alternate Dielectrics

The thermal conductivity of the buried oxide is almost 100 times smaller than that of Si. Therefore, local self-heating in SOI can be a concern for devices that are used in the on-state most of the time, for circuits with a high duty cycle, and for bipolar ICs. Scaling the Si film thickness degrades the thermal conductivity and increases the thermal resistance, with thin Si and thick BOX as the worst case.[51] A simple countermeasure is to scale down the BOX thickness. A factor of three improvement in thermal conductance can be achieved by reducing the BOX thickness from 150 nm to 20 nm.[52] The tradeoff is, of course, increasing the parasitic capacitances and reducing the overall device performance. Another approach is to introduce a high

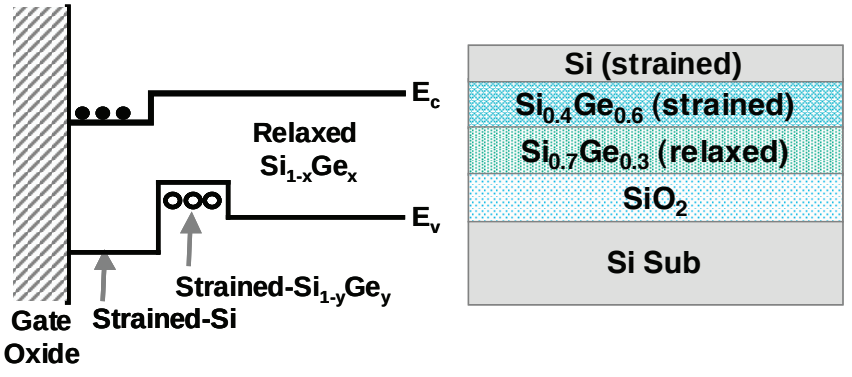

FIG. 8. Schematic layer structure and band diagram for a dual channel device that is based on strained Si deposited on top of strained SiGe (after Ref. 43 and 44) .

thermal conductivity material as the buried dielectric. There are several options[52] but silicon nitride appears to be the most attractive one. It is an industrially mature material, it exhibits an order of magnitude higher thermal conductivity than SiO_2, and it is a well-characterized insulator. It has been shown that a composite nitride/oxide buried dielectric, as shown in Fig. 9, is a viable approach for an improved thermal conductivity substrate.[53]

In contrast, if the focus is low power consumption, ultra-thin BOX is very advantageous. It offers the possibility to easily form buried n and p regions in the handle substrate as a back gate for low voltage operation and also for improved SRAM stability.

Self-organized Nano-Patterns Facilitated by Wafer Bonding

Precise misalignment of two crystalline lattices leads to formation of controlled and regular networks of dislocations. Figure 10 shows an example of a 2D dislocation array obtained by bonding two Si (100) wafers with a small twist angle between the top and bottom wafer.[54] The dislocation arrays induce 2D periodic strain fields at the surface of ultra thin Si bonded layer and can be used as the template for nano-organization of subsequent processes, *e.g.*, nanogrowth of Ge quantum dots, memory crystals, DNA cells. It is important to notice that layer transfer is a unique technique that allows nano-scale self-organization over wafer-size surface areas.

Some Unique Devices Enabled by SOI

SOI substrates are used in high volume manufacturing of microprocessors and "smart power" devices, are utilized in high voltage circuits, ultra-low power circuits, MEMS devices, and are entering the RF and photonics area. In addition there are some applications that would be almost impossible without SOI. We describe two such cases below.

Capacitor-less one transistor SOI DRAM.—Floating body effects result from the generation of excess charge in the SOI body, which change the channel potential. During high frequency operation, device charging and discharging leads to memory effects and, because of its iterative nature, to history effects. IC designers put special attention on the management of floating body effects to avoid noise and threshold voltage instabilities.[55] On the other hand, the floating body effect if well controlled can be used for data storing.

Capacitor-less one transistor DRAM cells are a new development which takes advantage of the floating body effect in SOI MOSFETs.[56-58]

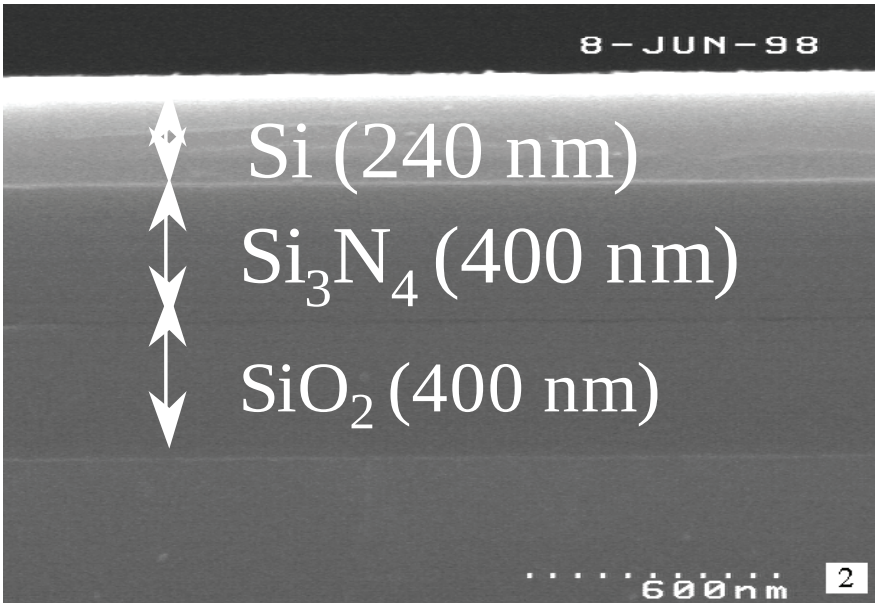

Fig. 9. *SEM micrograph of a composite nitride/oxide buried dielectric under a silicon film.*

The generation of excess negative or positive charge in the body can be used to store data states as illustrated in Fig. 11.[57] In an n-channel device an excess of positive charges leads to an increase of the current drive, defining state "1". The removal of positive charges from the body decreases the channel current, defining state "0".[56-60] The strong industrial potential of the floating body cell (FBC) comes from the fact that very dense embedded memory blocks can be realized with a standard SOI process, with a memory cell footprint that is approximately one half of that of an embedded DRAM.[61]

Taking into account that embedded memory occupies more than 70% of today's microprocessors[10,55] FBC

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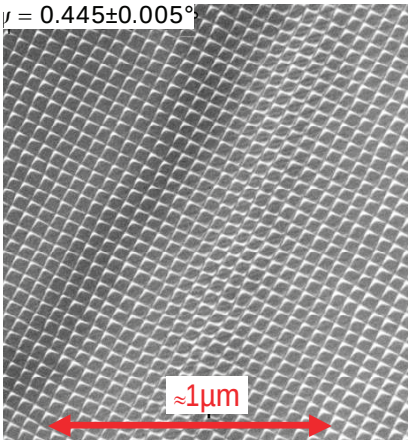

Fig. 10. *A two-dimensional dislocation array obtained by bonding two Si (100) wafers with a small twist angle Ψ between the top and bottom wafer (from Ref. 54).*

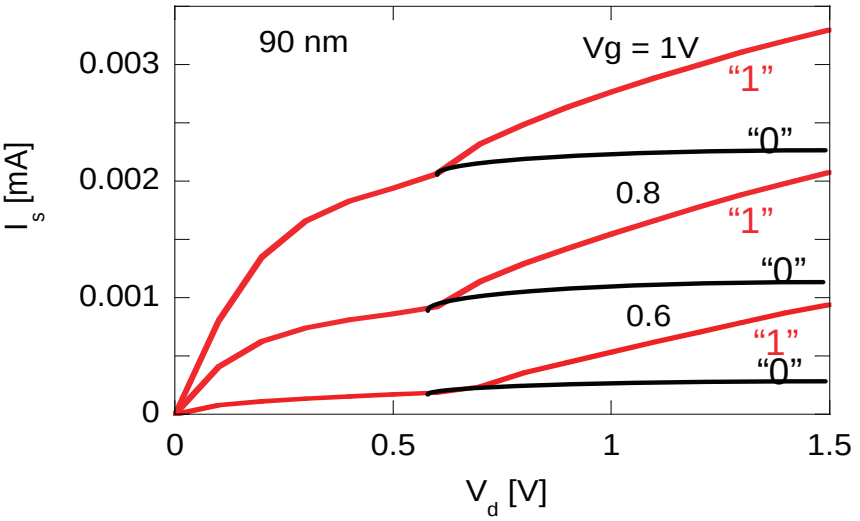

Fig. 11. *Electrical I-V curves of a floating-body SOI transistor depend on the charge that is present in the body. This can serve to store memory bits (from Ref. 57).*

embedded memory will allow for a reduction of the overall die area or the addition of significantly more memory at constant die area.

FinFETs and other multigate transistors.—Multiple-gate FD transistors provide better electrostatic control in the device channel than is possible with traditional single gates. Three-dimensional structures known as FinFETs after the "fin" like shape of the silicon channel are a major innovation in the device architecture. There are several types of FinFETs as schematically shown in Fig. 12. FinFETs were first proposed in the late

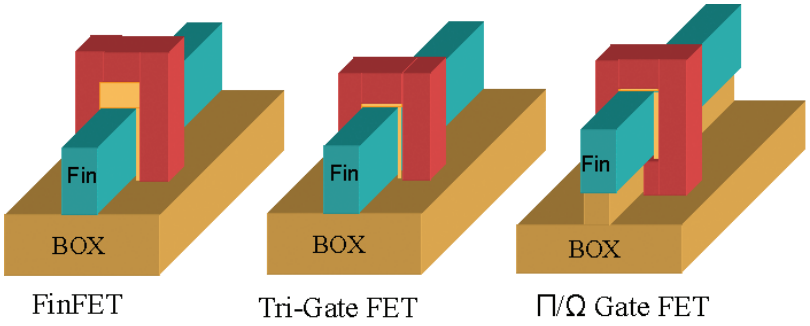

Fig. 12. *Three configurations for a Fin-based multi-gate transistor.*

'80s[62] but their advantages have only become relevant in the sub-45 nm device generation. A key element in the manufacturability of these new devices is the SOI substrate. The Si layer thickness becomes the fin height and defines the transistor width. A controlled undercut of the BOX after fin patterning defines the Omega-FET. The buried oxide can also act as an etch stop, although in some cases a composite dielectric nitride/oxide, like the one shown in Fig. 9, can further improve the etch stop efficiency and will avoid dielectric undercut during H_2 smoothing of the FIN lateral roughness.[63]

Conclusion

Current and future transistor scaling heavily depend on ever more advanced engineered substrates. As we move deeper into the nanotechnology era, the symbiotic relationship between the substrate engineering and the device design will only grow stronger. Demands of future circuits will continue to drive the development of specialized engineered substrates. Mobility enhancing substrates will play a key role for the 45 nm technology node and beyond.

SOI, which is already in the mainstream for high performance microprocessor applications, will continue to extend its range of applications. Smart power applications, particularly for automotive use, are growing. High resistivity SOI substrates gain interest for RF and SOC applications. The ultra thin buried oxides are a feature that allows the integration of a back-gate for dynamic threshold voltage control. Integration of embedded one-transistor floating body memories on SOI will result in ICs that will have speed and power advantages at a significantly lower cost. When transition to fully depleted multi-gate devices occurs, SOI will be the key element in ensuring that these 3D structures, such as FinFETs, are manufacturable. SOI substrates are used for many types of MEMS and are gaining importance in photonic applications thanks to the excellent waveguiding properties of the Si layer on SiO_2.

Monolithic integration of dissimilar materials, such as GeOI, but also GaN on Si or Si on poly-SiC, will enable future electronic, optoelectronic and photovoltaic applications, while controlled defect arrays will contribute to the advancement of self-organizing nanostructures. ■

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