Advances in Ultra Low Dielectric Constant Ordered Porous Materials

by Richard Farrell, Tandra Goshal, Uros Cvelbar, Nikolay Petkov, and Michael A. Morris

Modern computer processors are fabricated in numerous process steps that can be conveniently described as front end (i.e. logic device level) and back end (interconnects, vias, and packaging).[1,2] Until recently, electrical isolation at the device and the interconnect was achieved using silica. This was either thermally grown (device layer) or deposited by CVD (interconnects). The unique role of silica as the universal isolation material ended with the advent of new high dielectric constant (high *k*) materials such as hafnia where the increased dielectric constant (which increases the capacitance of the device compared to an equivalent thickness silica gate) is balanced by a thicker dielectric layer thickness.[3] This increased thickness reduces current leakage to minimise power usage. The high *k* and low *k* materials have quite different functions in modern logic devices. The high *k* material aims to allow a field to be generated at the surface of the device channel while minimizing gate leakage. On the other hand, the low *k* material has the almost opposite aim– to minimize field penetration between conductor elements.[4-6]

The low *k* materials used are being constantly optimized to address two important issues: (1.) to prevent leakage between wiring elements of the circuitry,[7] and (2.) to minimize time delay losses in the wiring.[8] Time delays arise from parasitic capacitance deriving from the proximity of the wires and inter-wire field penetration. Resistive-capacitive (RC) coupling effectively increase the time taken for electrons to pass through the circuit.[9] The delay time can be approximately written as[8] follows

$$\text{time delay, } t_{RC} = 2\,\rho k \varepsilon_0 (4L^2/P^2 + L^2/D^2) \qquad (1)$$

where k = the material dielectric constant (or relative permittivity) , P = wire resistivity, L = wire length, P = metal pitch, and D = the wire height. The time delay can be compared to the gate delay time, which is defined by the time it takes to charge the logic device. As devices have been miniaturized, the gate delay has continually decreased because the charge needed decreases with size while the RC related delay has increased because pitch and diameter of wires has decreased.[10]

Figure 1 shows the relationship of gate and RC delay as a function of the technology node (feature size). It should be noted that power issues are of least equal importance as delays in design and fabrication of nanocircuitry.[1,2] Power inefficiencies arise from simple current drains but also from parasitic capacitance (described above), which ensure that extra current is required so the parasitic capacitors can be charged/ discharged. The parasitic capacitance is highly frequency dependent and increases with the period over which voltage change is reduced. Moving toward a low *k* material thus reduces parasitic capacitance, which in turn enables faster switching speeds, lower power consumption, as well as reducing time delays. Low *k* dielectrics also reduce cross talk noise which can cause spurious switching and failure in modern digital circuits.[11]

As can be seen in Eq. 1, this time delay can be reduced by decreasing *k* and the wire resistivity. There is little scope to modify the conductivity of the interconnect as copper has the lowest resistivity available of metals that are compatible with modern device processing. In a simple parallel plate capacitor the relationship of *k* to the capacitance, C, is given by

$$C = Q/V = k\varepsilon_0/d \qquad (2)$$

where ε_0 is the permittivity of free space (vacuum), C is the charge on the plates, V the applied voltage across them, A is their area, and d their distance apart. By decreasing *k*, the charge decreases lowering field penetration and reducing time delay etc. Low *k* materials can be divided into several classes.[6] Silica has a dielectric constant of 3.9 which is the lowest for any dense ceramic. Polymeric materials (Teflon, polystyrene) are usually lower with values down to half of that of silica.[12] Silsesquioxane (SSQ) materials have a 3D polymeric structure with a molecular formula $(R\text{–}SiO_{3/2})_n$ and can have *k* values of around 3 or lower.[13] Doped silicas where oxygen groups are replaced by fluorine (fluorinated silicate glasses, FSGs, or alternatively known as silicon-oxy-fluorides, SiOFs) or by CH_x units (silicon-oxy-carbides, SiOCs) can also reach lower values than pure silica at about 3.5 and 2.5 respectively.[6] With the exception of organic polymer systems (which are difficult to integrate into current damascene processing), substantially lower *k* values than 2.5 have to be achieved by the introduction of porosity since air has a dielectric constant close to unity.[14]

Porosity can be introduced into solids in three principle ways.[15] First, the formation of a random pore structure caused by incomplete densification of the material.

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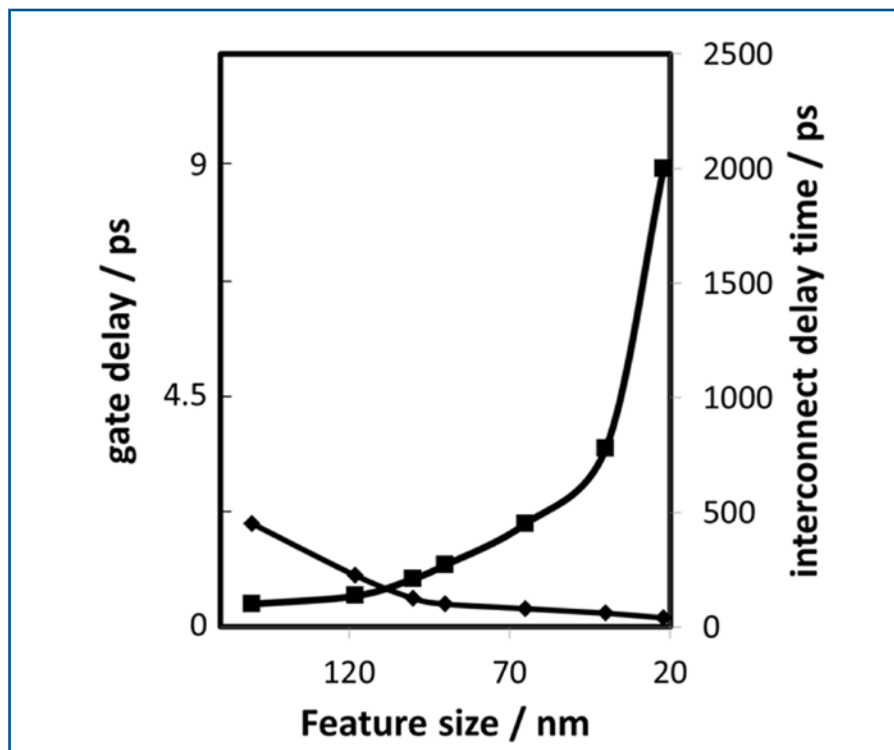

Fig. 1. *Gate delay (left hand scale) and interconnect delay (right hand scale) showing how the interconnect delay has become progressively more important as feature size has reduced.*

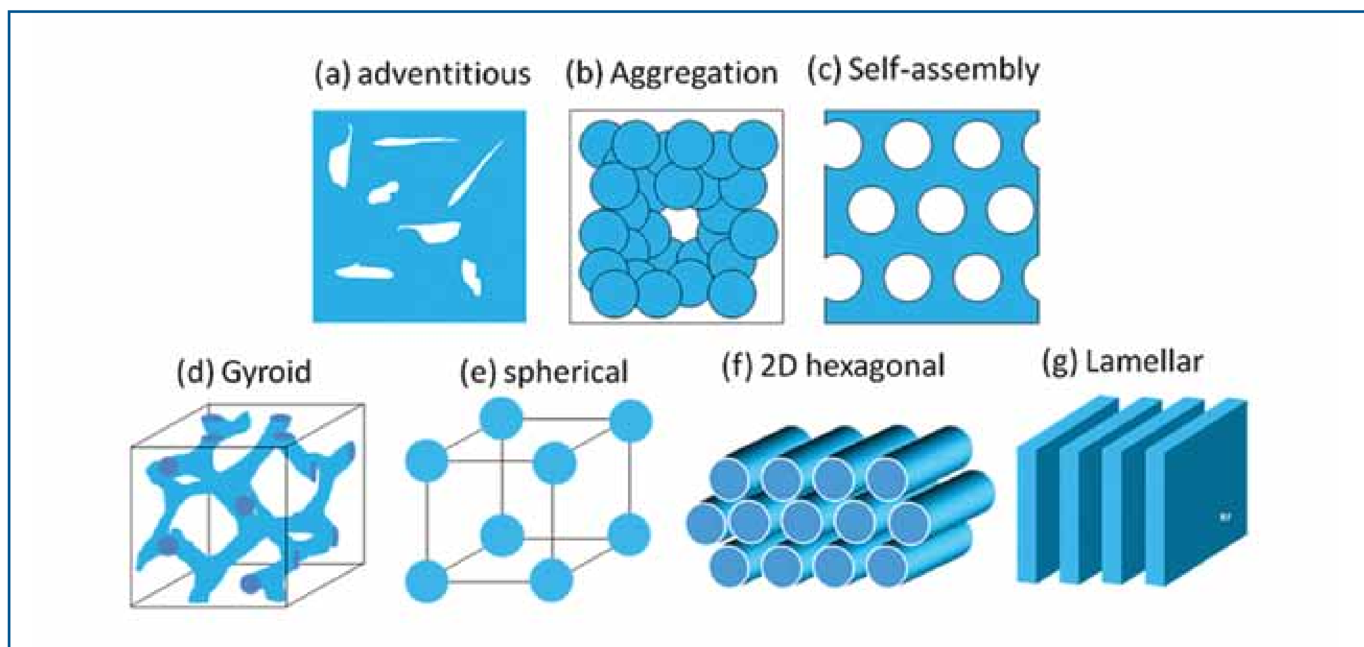

Fig. 2. *(a) to (c) types of pore systems. (a) is adventitious pores arising from sintering and densification as well as impurities. (b) pores formed by aggregation of particles. (c) pores formed via self-assembly. (d) to (g) pore arrangements seen in ordered mesoporous materials. (d) the gyroid structure, (e) ordered spherical pores, (f) the 2D hexagonal pore arrangement, and (g) the lamellar structure (darker color shows surfactant).*

Second, by inter-particulate voids formed between particulates and; third, where ordered pore arrangements are formed in the solid by careful chemical design (self-assembly). These are illustrated in Fig. 2. Since a ULK is defined by a *k* value of <2.5, it is necessary to have around >50% pore volume in a silica material if ULKs of less than 2 are to be achieved. In order to provide surfaces that are essentially dense and provide robust materials where large pores do not cause failure at low stress, it is almost a requisite to define a monodisperse pore size and a well-defined pore arrangement. Because of this, this article will focus on materials that have these types of structures.

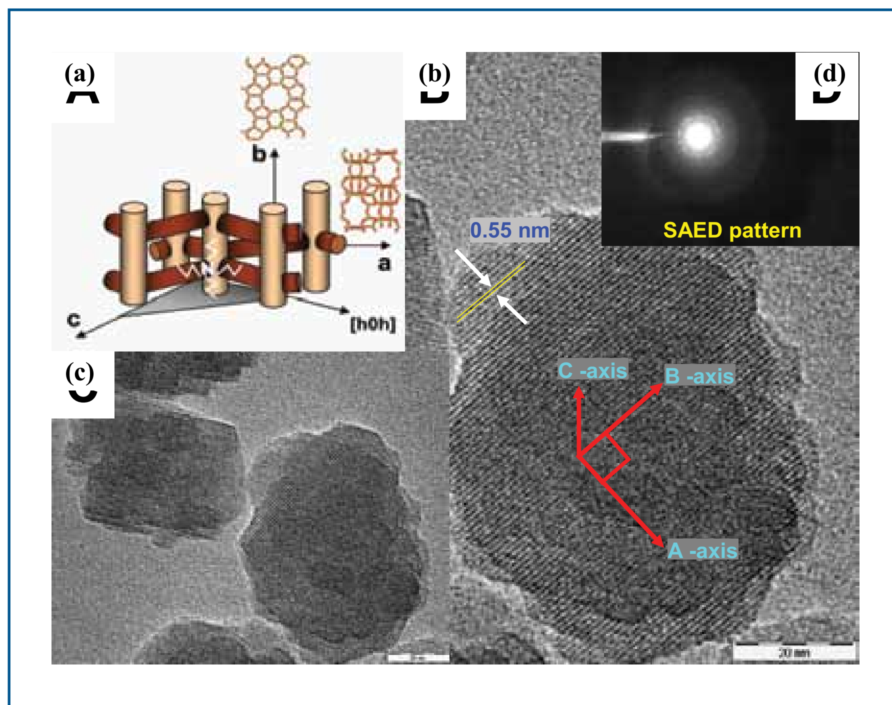

Fig. 3. *Structural representation (a) and TEM images (b and c) of the microporous silicalite-1 material (nanoparticles). The scale bar is 20 nm. The schematic representation shows the crystalline structure with the unit cell direction a, b, and c axis (perpendicular to plane of page) labeled. (d) is the SAED pattern for an agglomeration of nanoparticles showing the crystallinity.*

Microporous and Ordered Mesoporous Materials as Ultra-Low Dielectric Constant Materials

Microporous materials are a group of natural and synthetic alumina silicates (zeolites) that have small pores (usually less than 1 nm in diameter) as part of their crystal structure.[16] In synthetic systems, the highly ordered structures are usually formed by the use of a molecular template molecule which helps to direct pore formation. A typical microporous material is shown in Fig. 3. Ordered mesoporous materials do not occur naturally.[16] They are formed by the use of molecular templates (usually surfactants or amphiphilic block copolymers) where the copolymers aggregate into supramolecular micelle structures around which an inorganic precursor condenses to form an inorganic-organic composite.[17] The organic component is removed by calcination (high temperature anneal), solution (extraction), and UV degradation to leave an ordered porous network, the inverse of the micellar structure. Here, the pore size can be controlled between 2 and 20 nm by choice of templating molecules with different molecular weights or other methods.[18] Four principal pore arrangements can be defined: (1.) a bicontinuous cubic gyroid phase with a complex 3D network of pores, (2.) a cubic close-packed arrangement of spherical pore cavities, (3.) an hexagonal phase where pores form parallel arrangements, and (4.) a lamellar phase. The last structure is prone to structural instability during preparation (and is only stable while the surfactant

template is in place) and is not usually considered for the ULK application. The other structures have all been investigated to some extent. The spherical closed pore structure does offer advantages because it limits mass transport through the material and can afford increases in mechanical strength over random pore arrangements.[19] However, these have been largely ignored here because they are limited in terms of the maximum pore volume that can be achieved and reaching k-values < 2 is difficult.

Microporous zeolite thin films were first explored as ULKs by Yan and co-workers.[20] These films offer good thermal stability (i.e. no pore collapse or unidirectional shrinkage) and interparticle mechanical strength. They can be prepared via a simple spin-on method[19,20] or by in situ growth.[19,21] With simple spin-on methods a dispersion of small zeolite particles are prepared and cast onto a surface. Porosity originates from the interparticle porosity within the zeolite nanoparticles and the intra-particle porosity owing to the packing of the near-spherical nanoparticles in thin film format. Typical images of collections of the particles are shown in Fig. 3 and Fig. 4a. In order to produce reasonable films, good particle size monodispersity is required. These films demonstrate well-defined micropore size and porous (intraparticle) architecture and have demonstrated low dielectric constants of as low as about 1.50 (infinite frequency[20]). However, the use of these films is somewhat problematic despite their k-value and good heat transfer properties (important in use because of operating temperatures reached). Great care in preparation is required because the films are aggregations of particles and large particle size variations can result in poor overall mechanical strength, low breakdown voltages/current leakage, and high surface roughness.

A typical cross-section of a zeolite film is shown in Fig. 4 and shows the sort of roughness that can be obtained. Some of the zeolite work has suffered because authors have centered on simple measurements of dielectric constant (i.e. CV measurements) and ignored the probably just as important current-voltage characteristics. One of the more promising and thorough zeolite research studies has shown good leakage/breakdown characteristics coupled to a low k value (1.96); but here a surfactant template was used to add mesoporosity to the zeolite crystal structure and the surface was subject to organic termination in order to control the effects of water adsorption, which is deleterious to good electrical performance.[22]

The microporous particle films so show significant interparticle mechanical strengths of >100 GPa (compared to dense silica with about 75 GPa.[23,24] Unfortunately, zeolite films suffer from a variety of problems arising from the particulate nature and the unwanted large diameter, non-ordered mesoporosity caused by irregular nanoparticle shapes. Nanoindentation studies of zeolite films highlight their extemely poor mechanical strengths. Figure 5a displays modulus and hardness values for a 600 nm film (around 0.1 and 0.1 GPa respectively) while Fig. 5b shows the post nanoindentation AFM analysis. The lack of the interparticle strength is evident as the zeolite nanoparticles are easily forced aside to form ridges (highlighted by red arrows). Furthermore, the zeolite films have very poor adhesion to the silicon substrate as confirmed by their failure of the tape adhesion test in Fig. 5c. Particle size of the crystallites may also be a problem as feature size dimensions approach 16 nm and below. There is a tendency to form voids in these particulate films[25] and this can result in poor cohesive strengths.[26] Therefore, these films present an enormous integration challenge for high-volume manufacturing. Non-uniformities within films results in poor etch rates/variations, difficulties at chemical mechanical planarization (CMP) steps and interconnect misalignment problems. The films have high surface roughness that is difficult to reduce/planarize as polishing will generally result in pull-out of individual nanoparticles. Furthermore, the interparticle voids will also become problematic during the ICP patterning of the dielectric layers and also at the seeding barrier layer integration/gap fill steps.[27]

One approach to improve the materials is through using zeolite particles as a component of a composite matrix. The

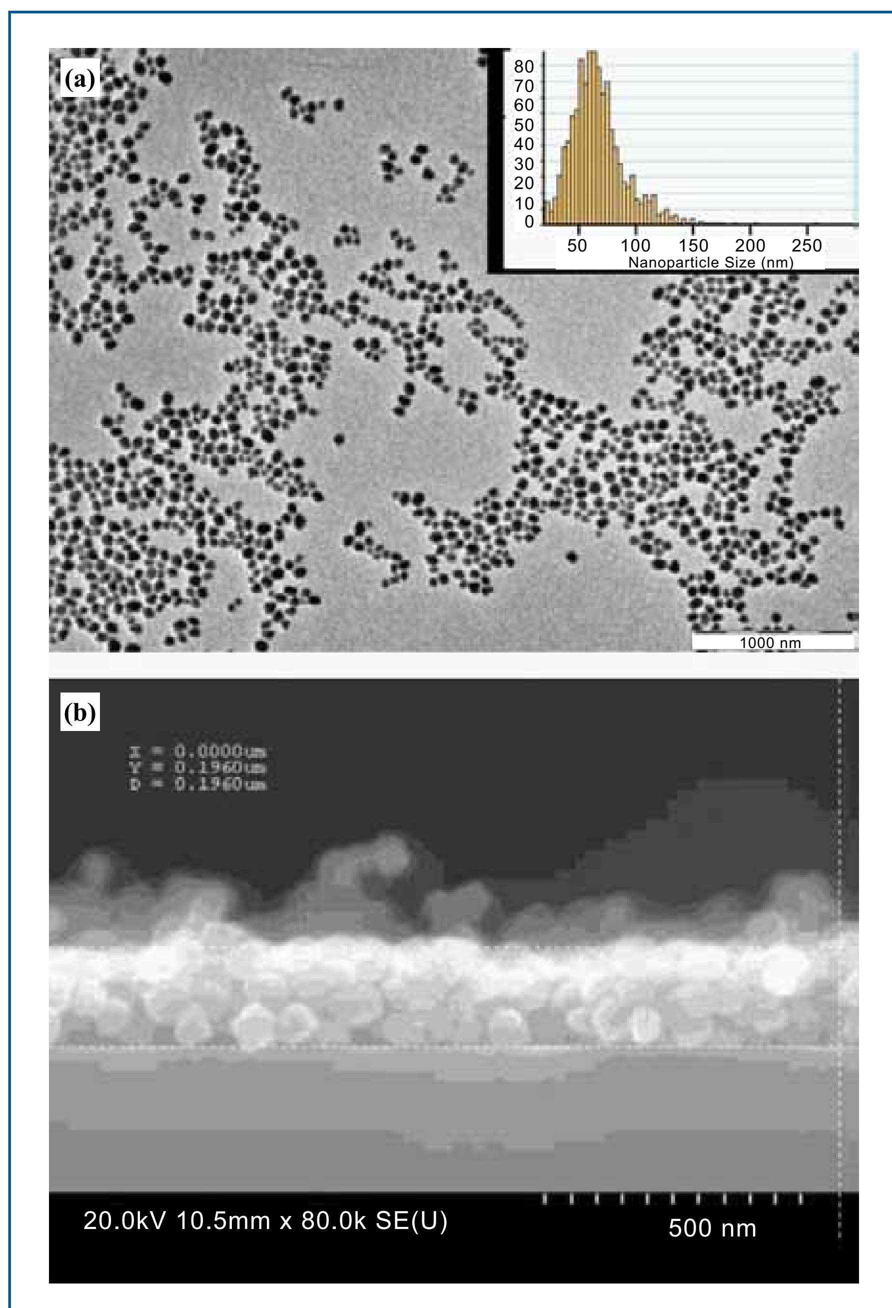

Fig. 4. *TEM image of zeolite silicate-1 particles (top image) and a SEM cross-section of a spin-coated film on a silicon substrate. The inset of top image shows the particle size (here measured at 60 nm) dispersion need to generate reasonable quality films.*

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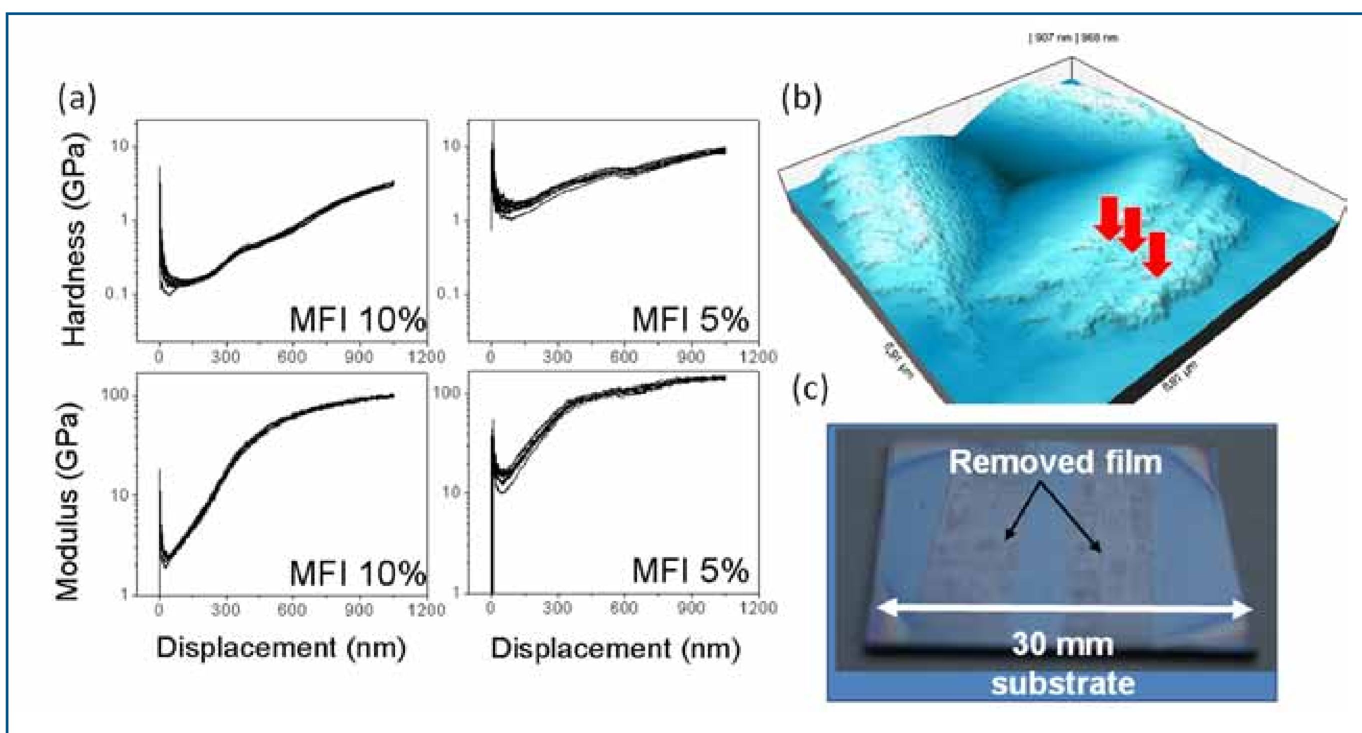

Fig. 5. *Nanoindentation studies of zeolite films: Hardness and modulus values for MFI 10% (600 nm thick) and MFI 5% (200 nm thick) microporous films. (b) AFM 3D topographic images of an indent taken after the measurement for a MFI 10% (600 nm) microporous film. The degree of pile up at a depth of 500 nm is 250 nm. The red arrows indicate the individual embankments. (c) Optical image of a silicalite-1 microporous film following tape adhesion testing. The film has been completely removed.*

addition of a dense tetraethoxyorthosilane (TEOS or similar) binder material enhances the adhesion of the film to the silicon substrate and removes the large mesostructural porosity by filling of void space; but this results in an increase of the dielectric constant because non-porous silica is being added.[26] Eslava *et al*. have used a similar approach and produce a composite film with 5 nm sized zeolite particles.[28] They also used a UV-cure means to harden the as-synthesised films and this allowed the film to remain hydrophobic whilst pendant $-CH_3$ groups on the amorphous silica component allowed the dielectric constant to be reduced to around 2.2. However, leakage currents were not reported. Industrially, there has been much interest in examining zeolite-CDO composites.[29] CDO (carbon doped oxide) is the basis of current industrial processes and is a silica material doped with carbon groups that is prepared via plasma-enhanced chemical vapour deposition (PE-CVD). Although the electrical improvements are quite modest, it does allow *k* values of <2.5 to be reached with improvements in mechanical properties over conventional films.

To improve the dielectric properties further, work has shifted toward investigating binder materials with low permittivities. Polymers are promising in this respect because of their low inherent *k* values approaching 2.0 and hydrophobic properties that limit water adsorption and compromise of the dielectric properties. However, the challenge in their use is their low thermal robustness particularly low softening temperatures. Addition of a polymer binder material was previously demonstrated by Li and co-workers where 5-15 wt.% of c-cyclodextrin was added to promote adhesion between the nanoparticles.[30] The authors reported little loss in mechanical properties while maintaining a low dielectric constant. Larlus and co-workers have also reported the use of silicalite-1 zeolite films covered in an acryl latex layer to enhance mechanical properties and reduce surface roughness.[31] A dynamic dielectric constant ranging from 2.1 to 2.4 was reported but this was via spectroscopic ellipsometry rather than a direct capacitance-voltage (CV) measurement.[31] An overview of this zeolite polymer composite area has been given by Lew *et al*.[32]

A final approach has been reported by this author and co-workers where low *k* mesoporous materials are combined with zeolite nanoparticles; this approach is described below after a discourse on the mesoporous materials. The ordered mesoporous materials described in brief above were first synthesized in ground breaking work by workers at Mobil.[33] They differ from the microporous materials in many ways but a major difference is that these silica films are comprised of amorphous silica and there is no crystallinity in the materials (although the pore structure can provide strong X-ray scattering and diffraction peaks). The practicality of these materials in thin film form advanced with the use of tri-block amphiphilic and other surfactants[34] and high quality film production became commonplace.[35] Provided the necessary care was taken, these films were well-adhered, of regular thickness, and crack/particulate free.

A typical example of a well-ordered mesoporous film formed using a tri-block polyalkene oxide surfactant template with hexagonally arranged pores is given in Fig. 6. However, these films are unlikely to exhibit this perfect structure through the entire film and commonly exhibit a poly-grain structure with various structural defects.[36] Often, because of solvent evaporation rates that vary as the solvent front moves through the film during preparation and drying,[37] the films can exhibit a central portion that has a disordered worm-hole type porous structure but are well-ordered at the air and substrate interface (Fig. 6). These data are discussed in depth elsewhere.[38] In order to understand how the dielectric properties of the films can be controlled by the structure of the film, it is obviously necessary to carry out exacting studies of the pore structure and pore size. Clearly, the total pore volume relative to film volume should be as high as possible to ensure the lowest possible dielectric constant and it should be noted that small micropores will also contribute to the lowering of the *k* value.

There has now been a considerable amount of work reported in the literature. However, many of the reports have been flawed by poor electrical measurements measured by optical and other indirect methods or with no leakage or breakdown characterization reported. The Pluronic F127 templated films (Pluronic is a trade name of a tri-block polyalkene oxide surfactant with the number code indicating the composition) have been studied by Morris and co-workers and these authors emphasize the need for very careful electrical characterization.[39] The films exhibited remarkably low level leakage currents (10^{-7}-10^{-8} A/cm^2 at 1 MV/cm^1) and high breakdown voltages (>3 MV/cm^1). The films also have dielectric constants of approximately 2.3, low dielectric loss factors of 0.01-0.03, and exhibit negligible frequency dispersion of dielectric constant between 100 kHz and 1 MHz. Other literature values for dielectric constants by electrical methods of Pluronic templated films have varied considerably with measurements as low as 1.45 and as high as 2.6 reported.

Zhao and colleagues produced mesoporous films with dielectric constants between 1.45 and 2.1 using very large pores (10 nm).[40] Pai achieved dielectric constants as low as 1.8 using the pre-organized supercritical fluid template approach with Pluronic F127 surfactant.[41] Jiang *et al*.[42] measured cubic mesoporous silica films templated with Brij 56 (a polyalkane-polyalkene oxide block copolymer surfactant) and reported a value of 2.42 while Singh *et al*. measured values of 2.4-2.8 for Brij 56.[43] Kikawa *et al*.[44] reported a dielectric constant of 2.6 using a Pluronic P123 surfactant template while Yang and co-workers[45] measured dielectric constants as low as 1.5 and as high as 2.6 for the same template, but these authors were very careful to use carefully functionalized materials to control the properties of the films.

Yang *et al*.[46] reported a now widely accepted view that trapped water and surface hydroxyl ions. etc. within the films contributed significantly to the measured capacitance. These films are highly hydrophilic and their large surface areas ensure that water adsorption from ambient is rapid (as reported by Farrell *et al*.[39]). These authors minimized this effect by passivation using hexadimethylsilazane (HMDS) silylation of the silanol surface and this approach is now commonplace for protecting films during air exposure. The work of Singh and co-workers also emphasized the instabilities caused by physisorbed water on the electrical properties of Brij 56 templated mesoporous films. These authors showed that verified two thermally driven mechanisms were responsible: proton generation through fissure of silanol bonds and proton-induced passivation of dangling bond traps at the silicon interface during annealing. Under high moisture conditions, water will physisorb to silica surfaces *via* hydrogen bonding resulting in the release of mobile protons by silanol dissociation on pore surfaces (Grotthus mechanism[48,49]).

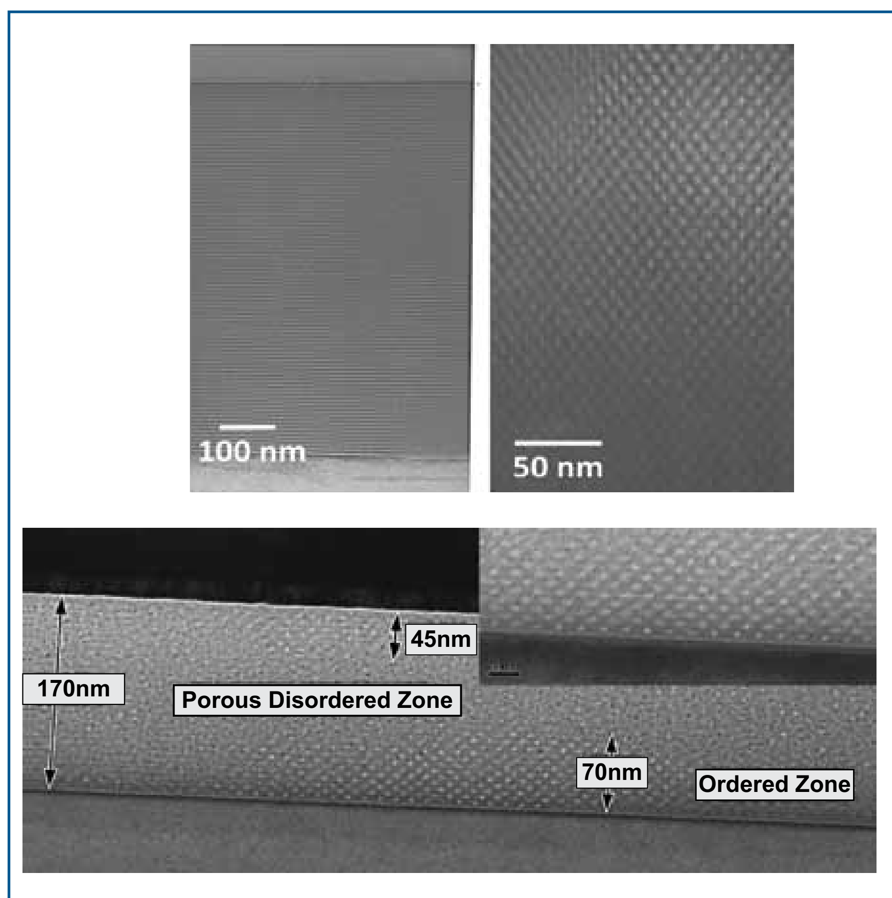

Fig. 6. *TEM cross-sections of mesoporous film. Top: An ideal structure viewed through plane parallel to pore direction (left) and plane perpendicular to plane (right). The pores are around 4.5 nm in diameter. Bottom: A film with a disordered central region. The pores are oval shaped due to in-film stresses.*

This reaction leads to changes in the flat band voltage. Furthermore, the surplus water forms hydrogen which can passivate the dangling bonds of silicon which act as the charge traps at the interface. Upon loss of water, the proton concentration decreases and the flat band voltage shifts in the opposite direction. In a later publication, the authors extended on their original work and revealed that these instabilities could be resolved by capping the silanol groups with trimethyl-silanes to limit proton conduction.[43]

It should also be emphasized that the electrical properties of the films reported can also be dependent on the characterization techniques and materials used. Fanga and Tsui[50] analyzed shifts in the flat band voltage of a porous silica material upon repeating measurements from accumulation mode to inversion mode and vice-versa with various barriers and contacts. They investigated the stability of the contacts/barriers and noted the change in V_{FB} was quite large when Cu was used in comparison to Al (confirmed by SIMS depth profiling). It is recognized that aluminium oxidizes at the silica interface and forms an alumina self-limiting barrier layer that impedes metal diffusion.

The presence of water and the characterization methodology are not the only reason for reported variations in the reported values of the *k* value in the literature. As mentioned above, the structure of the materials—i.e., the pore arrangement, the pore size, the density of pores, and the presence of small micropores—all have a profound effect because they alter the actual density of the film. Because of this the large variation in dielectric constant for the templated films can be attributed to the various preparation techniques and variable (spin-coating, dip-coating, choice of surfactant, drying periods, calcination temperature, reaction time, reaction temperature, concentration of reactants, etc.) used by each author resulting in various intrawall silica/pore distances (densities). Also, it must be remembered that the complex structure of the materials can be subtly altered by the strain in the films and interface effects as discussed above.

Morris, Farrell, and co-workers explored the practicality of making microporous zeolite films using mesoporous silica as a matrix material.[52,53] The mesoporous material acts as a binder, filling in gaps between the ~50 nm zeolite (silicate-1) particles and promoting adhesion between the particles and the substrate. On careful microscopic investigation three distinct pore size ranges can be seen in these composite

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films: microporosity arising from the zeolite structure, mesoporosity from the mesoporous structure, and finally a larger, macroporous structure arising from strain within the film causing pore merging. The dielectric properties measured were acceptable. The *k* values were around 2.2 and showed only small dispersions with frequency. Leakage currents were less than 10^{-7} A and breakdown voltages exceeded minimum standards. However, it was recognized that the surfaces were not smooth due to presence of protruding particles. Integration of these in a manufacturing process would be difficult because planarization of a hard particulate in a relatively soft matrix is difficult. The zeolite nanoparticle size must be reduced if such an approach is to become feasible.

In summary, these ordered porous materials do afford a means to generate good low *k* and ULK films. Industry could readily realize *k* values well below and around 2 by methods that could be adopted in industry. However, further very careful electrical characterization is required to allow them to be used and this is scarce. The number of studies where frequency measurements, current-voltage, breakdown behavior, and process-sensitivity are relatively few and work on how they might be integrated into a manufacturing process flow is very limited.

Closing Remarks and Outlook

Despite the fact that industry roadmaps have constantly demanded interconnect dielectrics with lower *k* values and the realization of ULK materials via designer porosity, these materials have failed to make the transition from research to manufacture. Several reviews of the need for ULK materials and the approaches used have been written.[6] What is apparent is that that scientists and engineers have failed to meet ITRS (International Technology Roadmap for Semiconductors) goals for many years. It is not the electrical properties of these materials that have caused this lack of progress; it is instead the physical properties of these materials. These issues are briefly summarized here.

Introduction of porosity is inevitably related to a decrease in mechanical robustness. Two issues are important. First, as the dielectric is weakened, the copper lines and vias are exposed to more stress and can deform and fail. Second, in the current damascene process, the dielectric is physically polished, and this technology has been carefully optimized to give low damage. The possibility of introducing a weak material as the dielectric does afford significant problems. However, recent work has shown that these materials can be planarized using standard equipment[56] and typical images of planarized mesoporous films are shown in Fig. 7. The materials appear to be stronger than might have been thought because of their honeycomb nature, which very efficiently spread stress through the entire material.

The presence of pores also leads to increased mass transport through the system. This affects the sensitivity of the materials to moisture as well as increasing sensitivity to impurity and copper migration/electromigration. To some extent, the mass transport can be alleviated by controlling pore direction, e.g., using pores that are parallel to the interconnect direction and pores that do not directly contact interfaces. Pore direction control has been demonstrated for mesoporous thin films when confined in trenches[57,58] and the graphoepitaxial alignment of the pores in channels discussed in depth.[59]

As discussed above, the propensity of these porous silicates to adsorb water and cause a significant worsening of the dielectric properties is a very significant problem. However, since passivation can lower sensitivities to moisture, a more immediate and potentially limiting problem is the probability of damage during etch processing.[60] This can lead to densification and increased dielectric constant.

Finally, ordered mesoporous materials are competing against the well-established technology of plasma-enhanced CVD.[6] PE-CVD has been used to generate polycarbosilane-based dielectrics with dielectric constants as low as 2.3.[61] This technique has also been used to generate a nonporous fluorocarbon film using a C_5F_8 precursor.[62] The dielectric constant of the films was reported as less than 2.0 and also exhibited low leakage current with good mechanical and thermal robustness. The other competitive technology is the so-called air gap methodology where the dielectric constant is reduced by the introduction of free-space between copper wires.[55] Air gaps can be introduced via two methods. The first is non-conformal CVD deposition on metal lines with materials between them partially or completely removed, and the other method involves the use of a sacrificial material between the metal lines. Air gap technologies have shown good initial promise.[63,64]

In this way, it is clear that ordered mesoporous materials to offer an opportunity to engineer low-*k* films with controlled porosity and electrical properties consistent with the extension of current integrated circuit manufacture to very small feature sizes. In terms of their ultimate dielectric properties, they may outperform

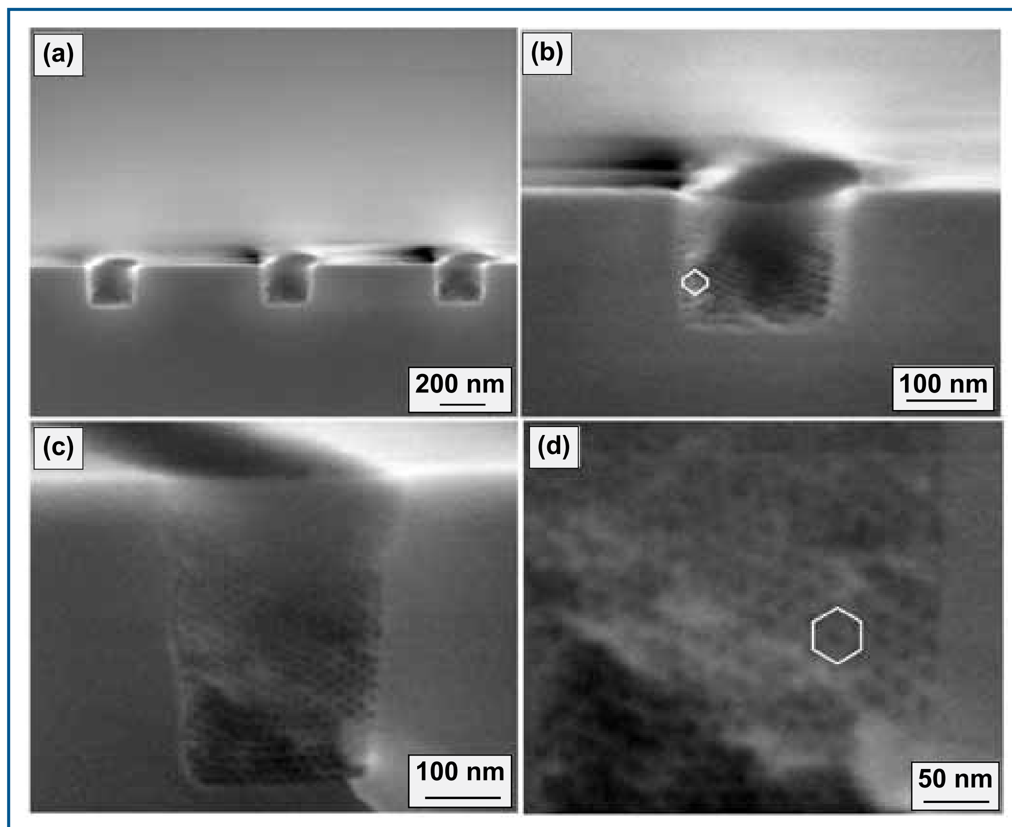

Fig. 7. *Typical images of spin-coated mesoporous films (cast into silicon topography) after mechanical planarization;[56] (a) is shallow trench image showing regularity and the surface that results from polishing; (b) is a close up showing the pore structure of the silica within the film; and (c) and (d) are images of deeper trenches.*

PE-CVD fabricated materials and thus they can provide a future solution to some of the roadblocks highlighted in the ITRS. Air-gap technology remains unproven for device manufacture and very significant challenges such as residual impurities, adhesion, copper strain, etc. must be addressed. However, until air-gap technology is proven for logic devices, ordered porous materials do afford a possible solution to development of ULK materials with dielectric constants well below 2.

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About the Authors

Uros Cvelbar received his BSc in physics and a PhD in materials science and plasma technologies from the University of Ljubljana, Ljubljana, Slovenia. Prof. Cvelbar is currently a Senior Research Scientist and Deputy Head in Department F4 at the Jozef Stefan Institute in Ljubljana, Slovenia, a professor at Jozef Stefan Postgraduate School, and teaches postgrad courses at different European Universities. Prof Cvelbar's interest of scientific research covers areas from materials science to plasma science, engineering, and technologies including nanotechnology, nanofabrication, nanostructures, and their applications. He works closely with industry and different scientific institutions worldwide. Prof Cvelbar is a member of the ECS DS&T Division Board. He may be reached at uros.cvelbar@ijs.si.

Richard Farrell received his BSc in chemistry (Honours) from National University of Ireland, Cork (UCC) in 2002 and his PhD in materials chemistry from the same institution in 2007. In 2007, Dr. Farrell joined Intel Ireland, where he was a research member in the Nanotechnology Group. From 2008 to 2009, he worked at CRANN and Tyndall National Institute where his role centered on developing novel lithographic approaches using self-assembly techniques. In 2009, he moved to the United States to pursue postdoctoral research on directed self-assembled of magnetic materials at the Department of Chemistry & Biochemistry and the Western Institute of Nanoelectronics (WIN) at UCLA. As of 2011, Dr. Farrell is a principal engineer at GLOBALFOUNDRIES working on advanced lithography. He may be reached at R.farrell@ucc.ie.

Tandra Ghoshal studied physics at Burdwan University, India and received a master's degree in 2002. She completed her BEd (Sc) from Burdwan University, India in 2004. She completed her PhD in materials science in 2009 from the Indian Association for the Cultivation of Science, Jadavpur University, India. During her PhD program, she worked on synthesis and characterization of some metal and metal oxides in one dimensional nanoforms. She is currently working as a post doctorate in the Department of Chemistry, University College Cork, Cork, Ireland. Her current research interests focus on self assembled diblock copolymer pattern formation for nanofabrication and nano-patterning of metal oxides on different substrates using diblock copolymer, their properties and application. He may be reached at t.ghoshal@ucc.ie.

Michael A Morris was educated in Liverpool receiving his BSc and PhD and from Imperial College London, Strathclyde University, and Cardiff University before moving to ICI. Prof. Morris is currently Professor of Inorganic Chemistry at University College Cork and leads the Nanoelectronics Project at CRANN in Trinity College Dublin. Prof. Morris's research centers on the development of self-assembly techniques such as microphase separation of block copolymers to create nanostructures and their application in electronics (both front end and back end) and other applications. Prof. Morris works closely with companies such as Intel, Millipore, and DePuy and successfully spun-out Glantreo, a company specializing in developing porous materials. He may be reached at m.morris@ucc.ie.

Nikolay Petkov received his MSc in chemistry from Sofia University, Bulgaria and his PhD in physical chemistry from the University of Munich, Germany. In 2005, Dr. Petkov joined the Chemistry Department of University College Cork, Ireland as post doctorate associate. In 2008, Dr. Petkov moved to Tyndall National Institute in Cork, Ireland as manager and chief characterization technologist of the Electron Microscopy and Analysis Facilities. Dr. Petkov's research focuses on advanced electron microscopy methods for analysis of self-assembled nano-structured materials, and nanowire-based devices and their applications. He may be at nikolay.petkov@tyndall.ie.

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