

High k Dielectrics on High-Mobility Substrates: The Interface!

by Durga Misra

The down-scaling trend of complementary metal oxide semiconductor (CMOS) field effect transistor (FET) will continue as it decreases the cost per function in a chip, decreases power consumption, and increases performance. To reduce power consumption from gate oxide leakage, Intel Corporation has successfully introduced high k dielectrics for 45 nm CMOS technology. We have, therefore, come a long way since a feature article on this topic was published in *Interface* in 2005.¹ Many deposition and reliability issues have been resolved on silicon substrate. To further enhance the performance and with recent advancement of high k metal gate technology, the semiconductor industry is again showing interest in high-mobility substrates such as Ge and III-V materials for CMOS technologies.²⁻⁵ Direct deposition of high k dielectric somehow reduces the burden of finding a stable oxide such as SiO₂ in Si. While Ge is being considered for high hole mobility, III-V materials such as GaAs, InP, InGaAs, InAs, and GaSb are being considered for their high electron mobility. Once these materials are integrated into the MOS device architecture, it will lead to a functional diversification with additional applications like high performance analog/RF devices.

According to the perspective on future evolution of CMOS technologies as presented at the International Technology Roadmap for Semiconductors (ITRS) (2010 edition)⁶ several critical issues need to be resolved before these channel materials are integrated into the CMOS device/process technologies. Several recent ECS symposia, "Dielectrics on Nanosystems,"⁷ "High Dielectric Constant and Other Dielectric Materials for Nanoelectronics and Photonics"⁸ and "Graphene, Ge/III-V, Nanowires, and Emerging Materials for Post-CMOS Applications,"⁹ have addressed these issues. First, alternate channel materials co-integrated with high k dielectric are required to implement high mobility n and p channels. Because III-V semiconductors have high electron mobility, (but low hole mobility), while germanium conversely has high hole mobility (but low electron mobility), selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers has become necessary. Second, formation of low-resistive source and drain with the allowed thermal budget is also required. Third, the channel structures may be different if the scaled device structures are modified to either FinFETs or nanowire structures.

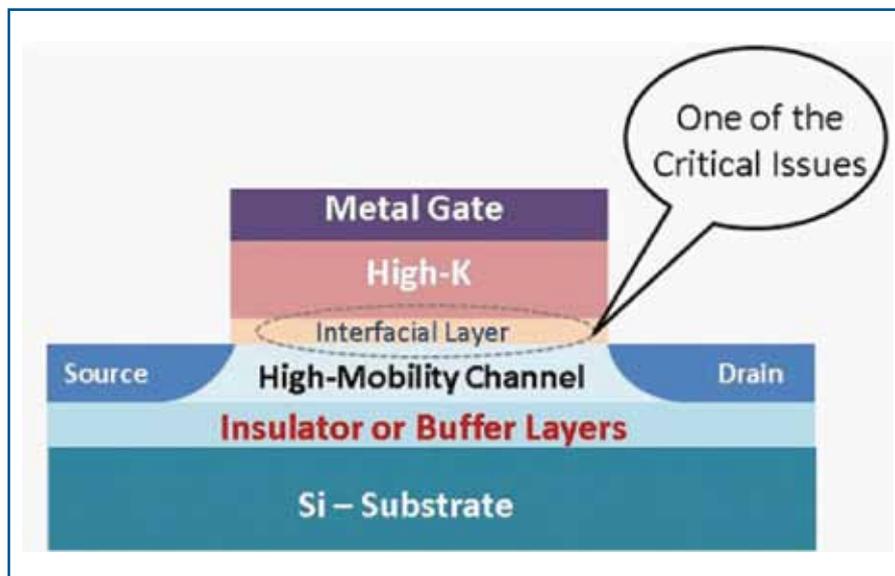


FIG. 1. The interface between the high- k layer and the high-mobility channel is one of the critical issues that needs to be resolved.

The other critical issue is the growth of high k dielectrics with an unpinned Fermi level in the alternate channel material. This issue schematically outlined in Fig. 1. Electrical performance of the high k /substrate interface depends on the deposition process, type of high k dielectric, and precise selection of deposition parameters, predeposition surface treatments, and subsequent annealing temperatures. Some types of dielectric materials may not easily nucleate in the same way on every type of substrate. Once the dielectric is deposited it may form a native oxide that could be detrimental to the electrical parameters of the interface. Pre- and post-deposition treatment may lead to different passivation mechanisms to improve the electrical properties. Unlike silicon, where the interface is well understood, the nature of the unpassivated dangling bonds may vary for various high-mobility substrates. Some of these interface states may be passivated by simple forming gas anneal or nitridation where others may require specialized passivation methods such as a-silicon, germanium or sulfur. Recent initiatives⁷⁻⁹ in this technology area outline the focus of current research to understand the interface states in high mobility substrates. Here some of the interface properties of high- k and the high-mobility channel materials are reviewed for both Ge and various III-V substrates.

Interface Electrical Parameters

The semiconductor-insulator interface is typically characterized by capacitance-voltage (CV) measurements of the MOS or MIS structure as a function of frequency and by analyzing interface state density (D_{it}). In the Si/SiO₂ interface silicon dangling bonds, the so called P_b centers mainly contribute to the interface states and are distributed in the silicon band gap. In high-mobility substrates such as Ge or III-V materials, on the other hand, the interface states originate from native defects that are not clearly understood. The distribution of these states is mostly collapsed to either conduction band or valence band depending on the semiconductor.^{10,11} A large density of interface states can cause Fermi level pinning. As the change of charge in depletion region due to external field or substrate doping is minimal because of interfacially trapped charge it leads to minimal band bending.¹¹ The interface state density can be estimated from CV or conductance measurements.¹² A modified Terman Method can also be used for calculating D_{it} for high-mobility substrates with high- k gate dielectrics.¹³ As the interface defect occupancy changes as a function of gate bias a stretch-out is observed in the high-frequency CV curve (Fig. 2). Frequency dispersion in accumulation and depletion regions in the CV curve is due to the strong presence of high interface state

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densities. A large inversion capacitance frequency dispersion is possible depending on the interface trap life-time.

High k/Ge Interface

The unstable native oxide on Ge was the biggest stumbling block in the past for very large-scale integration of CMOS devices in Ge. With high- k gate dielectrics the Ge/high k interface still remains a concern if the native GeO_2 is not controlled properly. During early stages, devices made by depositing HfO_2 directly on Ge demonstrate significant hysteresis, mainly due to the formation or growth of an unstable interfacial layer of GeO_2 during or after the HfO_2 deposition. Diffusion of Ge into HfO_2 is also a problem. To achieve excellent electrical performance of Ge devices with high k gate stacks rigorous interface engineering work has been carried out. For example, O_2 annealing of deposited HfO_2 on Ge formed a stable hafnium germanate layer serving as an oxygen barrier compared to GeO_2 . Even though it forms a thinner interfacial layer compared to silicon this layer contributes to high interface state density.¹⁴ When a thin GeO_xN_y film is deposited on Ge substrate prior to HfO_2 deposition, Ge p-MOSFETs showed a twofold enhancement in mobility but the interface state density still remained very high.¹⁵ Additionally, different gate stacks of Ge oxynitride (GeO_xN_y) using either thermal or plasma anodic nitridation^{16,17} or GeON with low temperature gate oxide was used to form Ge MOSFETs.¹⁸ However, these gate stacks are not very scalable.

In another example of interface engineering, surface-nitridation of the Ge substrates was done prior to HfO_2 deposition

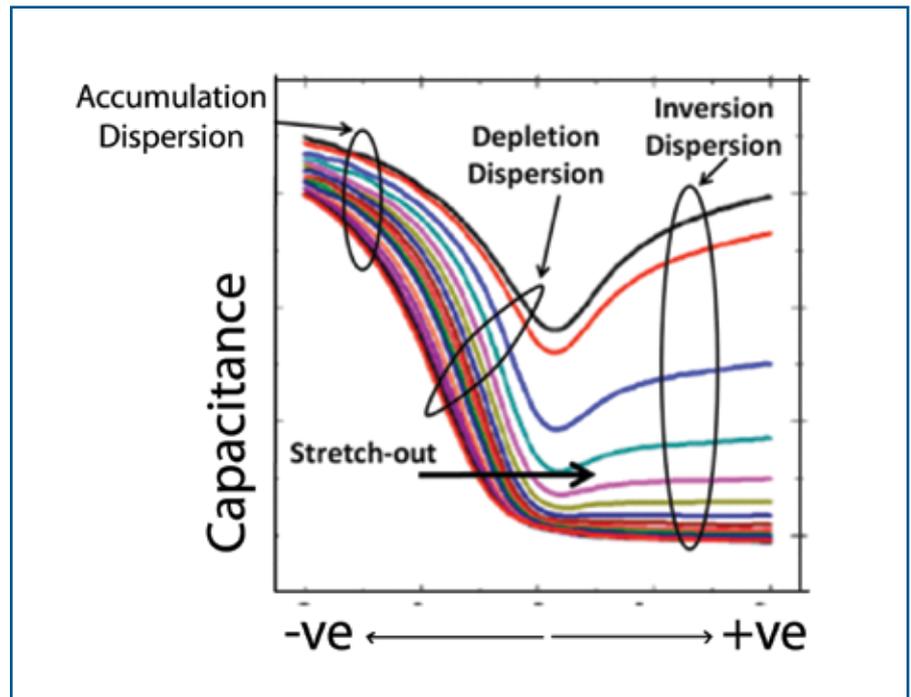


FIG. 2. A typical CV curve of high k on high-mobility substrate shows frequency dispersion in accumulation, depletion, and inversion region. A high-frequency CV curve stretch-out location is also shown.

by exposing the surface to an atomic N beam from a remote RF source.^{19,20} Significant dispersion in inversion region was observed for the nitrided sample as the frequency is reduced, indicating the presence of slow interface states. Similar dispersion was also observed by others²¹ in the inversion region on p-type substrate after the Ge surface was treated with O and N beams. It was concluded that the dispersion observed in the accumulation region as a function of frequency is mainly because of the series resistance effect. An increase was observed in the accumulation capacitance of nitrided

devices by a factor of 3 at high frequency compared to non-nitrided devices. This observation implies that surface nitridation improved the quality of the gate dielectric and possibly helped in restricting further growth of the interfacial layer²² but yet degraded it by introducing a large number of interface defects.

Surface treatment of Ge substrate prior to gate dielectric deposition seems to improve MOS device quality but it is not integration worthy. For example, Ge surface passivation was done by forming a thin Ge oxynitride film,^{23,21} by NH_3 annealing,²² by depositing

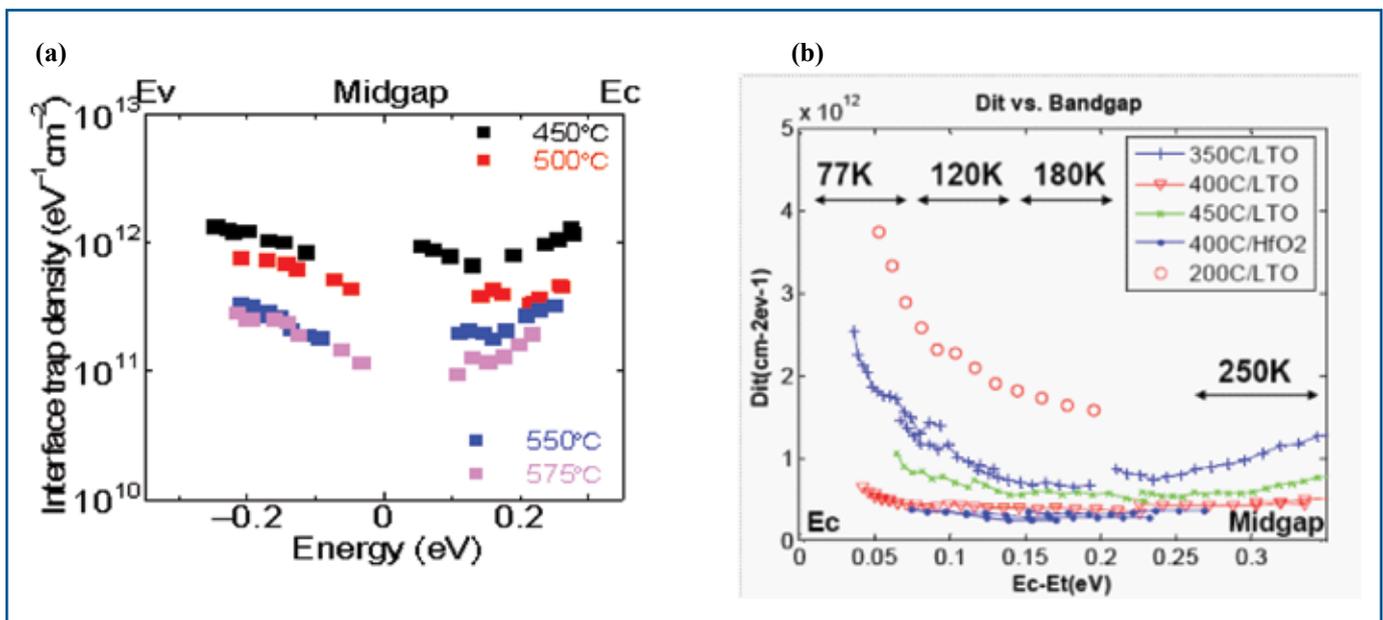


FIG. 3. (a) Energy distribution of interface state density, D_{it} is shown as a function of GeO_2 oxidation temperature²⁸ and (b) for ozone-oxidized Ge/GeO₂ interface.²⁹

Si and subsequently oxidizing it,²⁴ or by SiH₄ annealing.²² Ultra-thin SiO₂/GeO₂ bi-layer passivation was used to reduce the interface state density.²⁵ It was also demonstrated that initial treatment of Ge surface by atomic N beam seems to improve the physical and electrical characteristics of MOS capacitors.²⁶ In most of the cases the interface shows a high trap density (D_{it}) regardless of the surface treatment. Exploring the interface through electron spin resonance measurement resulted in no evidence of Ge dangling bonds at the Ge/HfO₂ interface and the dominant contributors to interface traps were the defect centers in the dielectric layer close to the interface.²⁷ It is, therefore, possible that the quality of the interfacial layer has significant impact on the interface state density and this notion has led to fine control the GeO₂ interlayer by thermally growing it.

Recently, it has been demonstrated²⁸ that when GeO₂ is grown on p-type Ge surface by thermal oxidation, an improved Ge/GeO₂ interface is obtained with a D_{it} of 10¹¹ cm⁻²eV⁻¹ without any annealing or interfacial passivation. As shown in Fig. 3a the interface state density decreased with an increase of oxidation temperature. However, when the temperature increased above 600°C non-uniformity in GeO₂ film was observed. In addition, to fabricate the transistor, a passivation or capping layer was required to protect the water-soluble GeO₂. Ozone-oxidized Ge/GeO₂ interface²⁹ also reduced the D_{it} as shown in Fig. 3b and once temperature increases above 400°C, D_{it} started to increase.

Theoretical calculation suggests that even if high-quality GeO₂ results when the high *k* dielectric is deposited, oxygen vacancies tend to migrate towards GeO₂ degrading the interface.³⁰ This further leads to the existence of doubly-occupied Ge dangling bonds near the middle of the Ge band gap.³¹ Incidentally, these were not detected by ESR because of their density lies below the ESR detection limit due to the viscoelastic properties of GeO₂. These defects may trap electrons limiting the performance of the device.³⁰

Various process optimization techniques are currently employed to make the interface superior. Excellent interface states were observed by scavenging the GeO_x layer from the interface by low-temperature annealing.³² On the other hand, a very short-term plasma oxidation through the high *k* gate dielectric suppressed D_{it} while maintaining an ultra-thin EOT.³³ Mobility enhancement in the Ge channel will be possible once the interface state density is significantly reduced and stable during normal operation. Given the above, it is imperative that a permanent solution with high quality sub-nanometer GeO₂ at the Ge/GeO₂ interface is required to integrate Ge into standard CMOS technology. Even though some works on negative bias temperature instabilities were reported,³⁴ the jury is still out on reliability concerns associated with this interface.

High *k*/III-V Interface

The high *k*/III-V interface is rather more complicated and generally leads to a high interface state density because of the intrinsic properties of III-V surfaces and the nature of their oxidation chemistry. For example, it is known that on a GaAs surface (As-rich) a complete monolayer of As cannot exist thermodynamically as relaxation of the As-dimer block is essential for As-rich surface stability.³⁵ During oxidation, electrically active interface defects can be formed that are attributable to the As-dimers.³⁶ This leads to a poor quality HfO₂/GaAs interface and an increased concentration of interface states with attendant Fermi-level pinning.

Figure 4 shows the high-frequency CV characteristics of n-MOS Ti-Au/HfO₂/GaAs MOS capacitor at different temperatures.³⁷ Strong stretch-out in the CV curves suggests that the device has a large concentration of donor-like interface states. As the temperature decreases from 298K to 150K the inversion capacitance decreases due to an increase in the time constant of the interface traps. Frequency dispersion in the accumulation region is typical of high *k* gate oxides on GaAs³⁸ and is due to the presence of As-O or Ga-O as an inhomogeneous layer at the interface. Interface traps are mainly responsible for dispersion³⁹ in the depletion region. The interface quality has been improved significantly since then. However, degradation of interfacial composition warrants a reliable interface passivation scheme on III-V semiconductors to eliminate or control Fermi level pinning.^{40,41}

Most of the recent passivation techniques show quality improvement but have some limitations. For example, incorporation of a monolayer of Si or Ge makes the interface⁴² robust but we are back to Si or Ge on III-V materials. Nitrogen or sulfur passivation is also used to improve the interface

characteristics.^{43,44} Variation of process conditions and low temperature oxidation at times make unpinning of the Fermi level possible. The Fermi level of HfO₂/In_{0.53}Ga_{0.47}As interface can also be unpinning by post-deposition forming gas anneal due to significant reduction in D_{it}.⁴⁵ Deposition of a monolayer of Al₂O₃ on In_{0.53}Ga_{0.47}As prior to HfO₂ growth resulted in an improvement of the interface and reduction in D_{it} due to removal of In_{0.53}Ga_{0.47}As native oxide in a so called self-cleaning process.⁴⁶

A combination of pre-deposition ECR plasma nitridation of InGaAs surface followed by post-deposition annealing significantly reduces the interface state density.²⁸ By employing a low-temperature plasma-enhanced-ALD (PEALD) Al₂O₃ on GaSb⁴⁷ an unpinned Fermi level was demonstrated in Al₂O₃/GaSb MOS capacitor as compared to regular ALD deposited Al₂O₃ on GaSb. Minimization of elemental Sb formation at the Al₂O₃/GaSb interface due to suppression of Sb₂O₃ reduction to metallic Sb results from the low temperature processing involved in PEALD⁴⁷ (Fig. 5). Sb₂O₃ reacts with GaSb forming Ga₂O₃ and elemental Sb and the kinetics of this reaction are suppressed once the temperature is reduced. Several such passivation schemes and process conditions are currently being applied to improve interface characteristics.

From the above few examples, the high *k*/III-V interface quality seems to be a function of surface chemistry, surface orientation of the substrate, and position of the electrically active defects on the band gap. Temperature measurements on MOS capacitors using high *k* on III-V are required to understand the mid-gap interface trap density. Use of high temperatures⁴⁸ and low temperature^{49,50} provides additional device information as the trapping predominantly occur at the interface.

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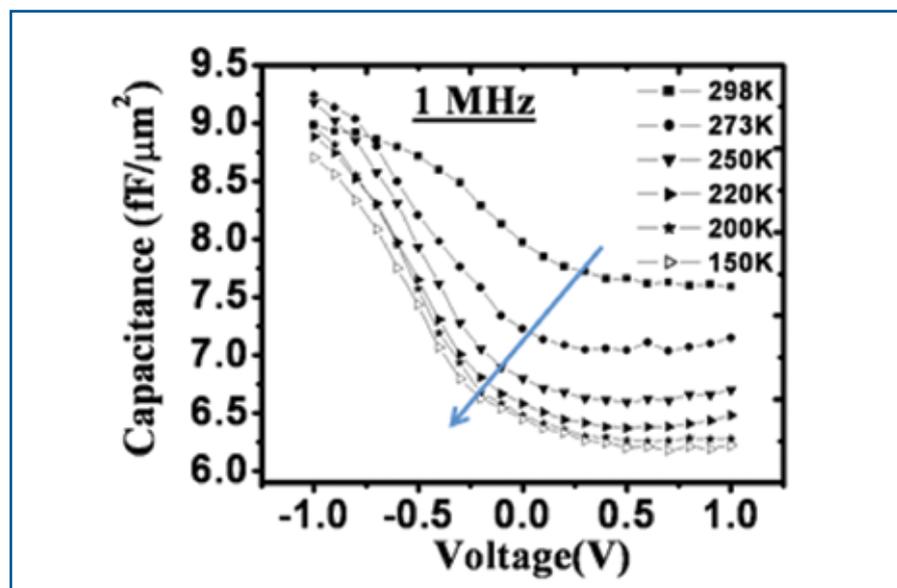


FIG. 4. High-frequency CV curves of TiAu/HfO₂/GaAs for n-MOS capacitor as a function of temperature showing large density of interface states.

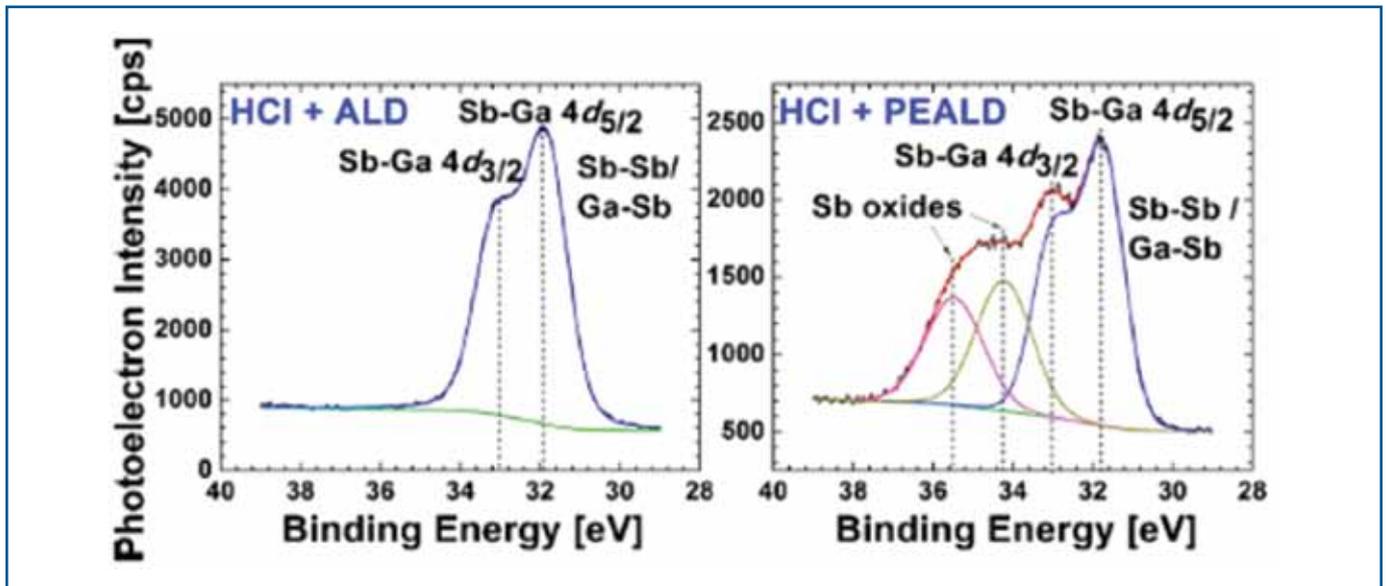


Fig. 5. XPS analyses of the Sb 4d region for ALD and PEALD samples show the presence of Ga-oxides. The ALD sample shows no evidence for Sb-oxides but PEALD samples have substantial Sb-oxides.⁴⁷

The D_{it} distribution in the band gap that determines Fermi level pinning is a result of unpassivated dangling bonds on the III-V surface and the defect generated during processing. These defects are typically due to the oxidation and consequent formation of electrically-active interface defects. An empirical model GaAs MOS structure reveals that the energy levels of interface states in the GaAs band gap (Fig. 6) that possibly dictate the extent of Fermi level pinning are at 0.75 eV and 0.5 eV and are due to missing As and Ga respectively.⁵¹ The first situation is associated with <111>A GaAs whereas the latter is typically noticed for the <100> orientation.^{51,52} The precise details of the exact location of the energy levels of a particular III-V compound surface depend on the processing details.³⁹ The physics related to III-V substrate and the surface chemistry is summarized in a book chapter.⁵²

Summary

The interface defect response at the high k and high-mobility substrate interface has been discussed in this short review. The impact of interface passivation techniques to optimize device performance was outlined. From the electrical performance, the interface characteristics seem to depend on the deposition process, combination of deposition parameters, the substrate surface orientation, pre-deposition surface treatments, and subsequent annealing temperatures. Some recent developments of the high k /Ge interface and high k /III-V interface and their characterization were discussed.

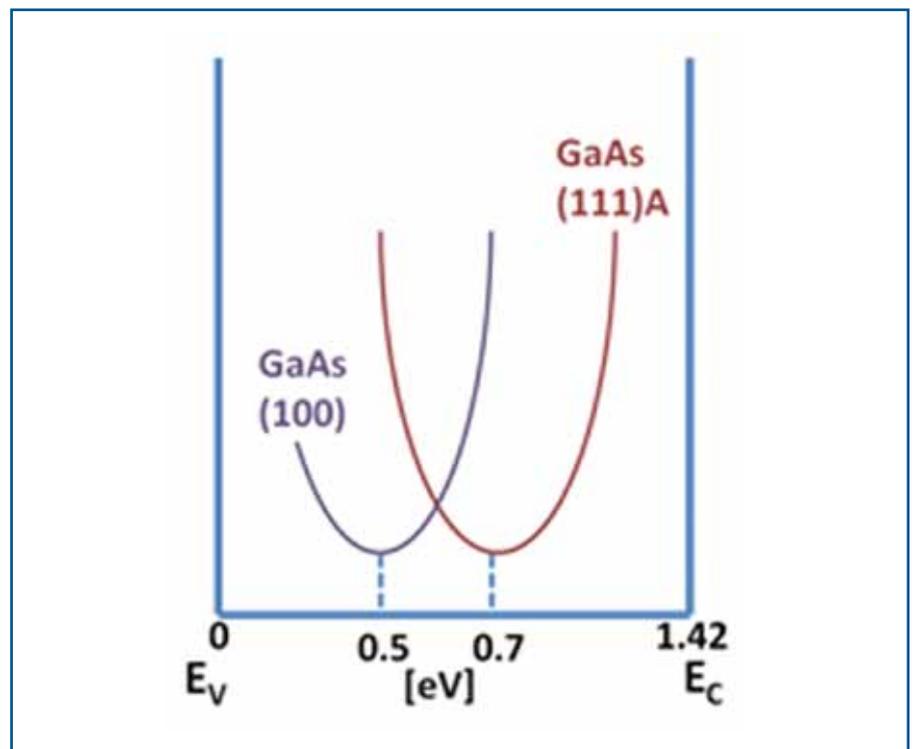


Fig. 6. The distribution and the minimum value of D_{it} depend on processing conditions.

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