Electrical and Reliability Characteristics of High-*K* HfO_2 Gate Dielectrics

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Abstract: As MOSFET devices are scaled down to below 100nm, the gate oxide thickness is required below 2nm. Conventional SiO_2 gate dielectric will be replaced due to excessive leakage and poor reliability. Thus, high dielectrics constant (K) gate dielectrics are being studied as an alternative. High-K dielectrics materials such as CeO_2, Y_2O_3, Ta_2O_5, HfO_2, ZrO_2, TiO_2, Al_2O_3, $SrTiO_3$(STO), and $BaSrTiO_3$(BST) have are studied[1-5]. Among them, HfO_2 is a promising candidate due to its thermodynamic stability on Si, high dielectric constant (∽25), and relatively large band gap (5.68eV).

In the paper, ultra-thin HfO_2 gate dielectrics films were fabricated, electrical and reliability properties such as capacitance-voltage (C-V), current-voltage (I-V), stress induce leakage current (SILC) effects and breakdown characteristics were studied.

In the experiment, HfO_2 capacitor samples have been fabricated using the following process. P-type (100) silicon substrates with 5-8Ω • cm resistivity were cleaned using H_2SO_4:H_2O_2 (2:1) solution and HF dip. Thin HfO_2 layers were following deposited at room temperature by ion beam sputtering a sintered HfO_2 target. Then they were annealed under various temperatures and ambient. After annealing, Pt top electrodes were deposited by sputtering. The area of the capacitors was $5\times10^{-5}cm^2$. The C-V and I-V curves were measured using HP4156B semiconductor parameter analyzer and Keithley590 C-V analyzer.

Figure 1 shows the capacitance-voltage (C-V) curves of HfO_2 gate dielectrics. The largest value of measured capacitance density in accumulation is $C_{max}/A=11.6fF/\mu m^2$. The equivalent oxide thickness (EOT) is about 2.9nm. Comparing capacitances of various annealing temperatures, the capacitance of the sample annealed at 400℃ is highest. With increase annealed temperatures, EOT increased.

Figure 2 shows the current-voltage (I-V) characteristics of HfO_2 gate dielectrics. The leakage current of the sample annealed at 800℃ is lowest, which is about $3.09\times10^{-6}A/cm^2$ at –1.5V gate voltage. No distinct SILC effect is obtained. The leakage current of the sample annealed at 400℃after $1\times10^6C/cm^2$ stress has a very little diversification. With increase annealed temperatures, the leakage current and SILC effect reduced.

Figure 3 shows breakdown characteristics of HfO_2 dielectrics. The breakdown electric field of HfO_2 dielectrics is more than $2\times10^5MV/cm$. With increase annealing temperatures, the breakdown voltages decreased.

Consequently, ultra-thin HfO_2 gate dielectrics (EOT<3nm) were fabricated. All samples annealed under various temperatures and N_2 ambient have good electrical characteristic and reliability. With increase annealing temperatures, EOT of increased, the leakage current and SILC effect reduced, the breakdown voltages decreased.

References:

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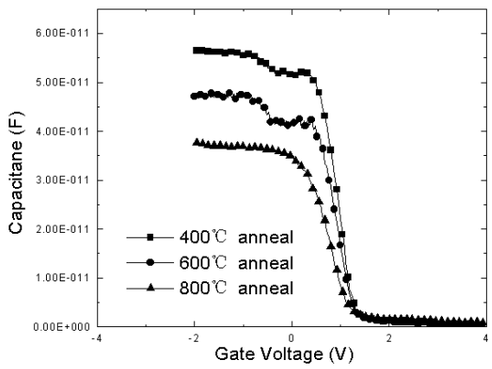

FIG. 1. C-V curve of HfO_2 at 400℃, 600℃, 800℃ anneal in N_2 ambient for 5min.

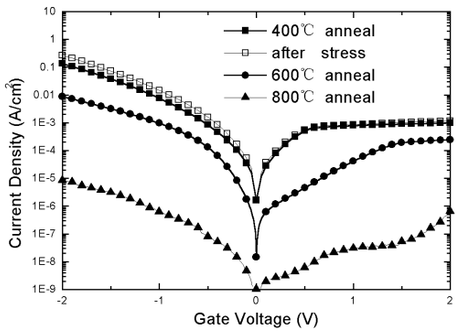

FIG.2. I-V curve of HfO_2 at 400℃, 600℃, 800℃ anneal in N_2 ambient for 5min, and after $1\times10^6C/cm^2$ stress at 400℃ anneal

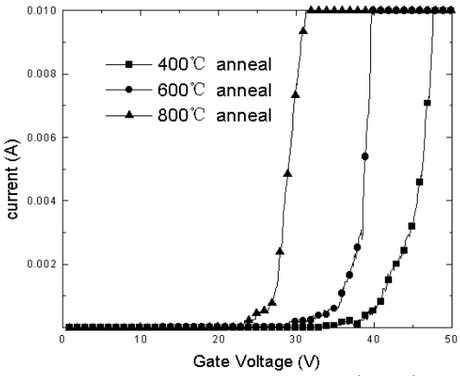

FIG.3. Breakdown characteristics curve of HfO_2 at 400℃, 600℃, 800℃ anneal in N_2 ambient for 5min