THE EVOLUTION OF PLASMA ETCHING IN INTEGRATED CIRCUIT MANUFACTURING

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The introduction of plasma etching methods into integrated circuit manufacturing began in the late 1960's and early 1970's. At that time the concept of etching solids by using atoms or radicals, created in a reduced pressure glow discharge, to react with solids to form volatile products was well recognized. Much of the early work was directed towards removing photoresists cleanly without affecting the underlying materials. The equipment that was used typically did not cause extensive energetic ion bombardment of the wafer surface. At this time, it was known that other materials such as Si, SiO_2, Si_3N_4, Mo, W and Ta could be plasma etched isotropically.

Although there was some discussion of profile control in this early work, it was not until plasma etching was carried out in capacitively coupled planar diode systems (early to mid 1970's) that it was realized that plasma etching had the potential to eliminate undercutting in the etching process. Within a very short time, the importance of energetic positive ion bombardment of the wafer surface was recognized by several groups around the world. However, the mechanistic aspects of this phenomenon were far from clear. Some years earlier, in studies of bias sputter deposition, the relationship between the geometry of capacitively coupled rf discharges and the plasma potential had been demonstrated. This work showed that systems in which the area of the powered electrode is comparable to the area of grounded surface in contact with the plasma (i.e., symmetric systems) will have very large plasma potentials. It was also known that, in capacitively coupled planar diode geometries, a more spatially uniform plasma density (and therefore a more spatially uniform ion flux) is obtained when the gap between the electrodes is much less than the electrode diameter (i.e., a symmetric geometry). Etching machines with this symmetric geometry quickly became popular. It was soon recognized that, in these symmetric systems, wafers placed on the grounded electrode were etched in a manner very similar to wafers placed on the powered electrode. This observation led to equipment with grounded wafer chucks. The high plasma potential in these symmetric systems causes energetic ion bombardment of all grounded surfaces. If some of these surfaces do not form volatile products upon reaction with species in the plasma (e.g., stainless steel), physical sputtering of these surfaces can occur. About this time, it was shown that severe micro-roughness of the etched surface can be caused when sputtered species are backscattered onto the etched surface. The need for a spatially uniform plasma with a low plasma potential led to the development of the capacitively coupled cylindrical diode (hexode) that dominated plasma etching until the advent of single-wafer processing. In this machine, the wafer area (inner cylinder or hexode) is always less than the area of the grounded outer cylinder (wall) resulting in a low plasma potential. During this time, particularly in Japan, microwave excited plasmas were being used for plasma etching processes.

Most of the plasma etching work at this time involved the use of halocarbon feedgases of which CF_4 was the most common. Early on, a very short but very important paper appeared in the literature that described a method to etch SiO_2 selectively to Si. This was needed for contact etching. The method involved using a fluorine-deficient (polymerizing) chemistry and was easily and quickly implemented throughout the world. Soon after, the importance of such polymerizing chemistries in controlling the undercut was recognized (sidewall passivation).

Although the importance of energetic positive ion bombardment of the wafer was recognized by many groups in the mid-1970's, the details of the surface science aspects of the process were not understood. The complexity of the environment in a reactive gas glow discharge impeded basic studies of the etching process. In the late 1970's, directed beam simulations of the plasma etching studies were initiated that allowed improved basic surface science studies, albeit in very much simplified conditions. These studies confirmed the importance of energetic ion bombardment in increasing the reaction probability of neutral species with solid surfaces.

The next issue in the equipment arena was the limitation that the capacitively coupled diode systems do not allow independent control of the ion energy and ion current density. A need to have fast etch rates with lower ion energies led to the introduction of planar triode etchers. At lower pressures, single frequency triode systems usually involve energetic ion bombardment of both powered electrodes often causing the micro-roughness mentioned previously. The introduction of dual frequency triode (and more recently, dual frequency diode) systems alleviated this problem. Near the end of the 1980's, systems using inductively powered sources to generate higher density plasmas, combined with capacitively powered wafer chucks to provide the optimum ion energy, were successfully introduced into the plasma etching equipment market.

Throughout the development of plasma etching equipment, there was a constant need to provide adequate cooling of the wafer. The heat load caused by the energetic ion bombardment and the exothermic etching chemistries can heat the wafers to unacceptable temperatures unless adequate cooling is provided. One approach was to inject some helium between the wafer chuck and the backside of the wafer initially accompanied by peripheral clamping of the wafer to the chuck. This helped but often led to a radial dependence of the wafer temperature causing a radial dependence of the etch rate. This problem was overcome by using electrostatic clamping of the wafer (i.e., the wafer serves as one electrode of a planar capacitor). This so-called electrostatic chuck (ESC) provides a uniform clamping force over the wafer surface and when this is combined with helium backside cooling, controlled and uniform wafer temperatures can be obtained in plasma etching environments.

Even when the plasma potential is low enough to eliminate wall sputtering as a source of contaminants, the reactor walls can play important roles in the etching process. Wall-catalysed recombination has long been recognized as a limiting factor in the transport of atoms and radicals at low pressures. This is a particularly important consideration in the design of chemical downstream etching equipment where the wafer is not in contact with the plasma. Furthermore, recombination of atoms/radicals on surfaces immersed in a plasma can greatly influence the steady state concentration of the atoms/radicals and the resulting etch behavior. The efficiency of this recombination process depends on the surface material, the surface temperature and the nature of the gas phase species. Recognition of these effects has led to chamber conditioning after a wet clean during which a clean, high recombination efficiency surface is converted to a slightly dirty, low recombination efficiency surface. Also temperature controlled (often heated) walls are now used to keep the surface processes constant during an etch run.