Electrodeposition of Through Chip Copper Plug for Three Dimensional Packaging

Kazuo Kondo[1]*, Jian-Jun Sun[1], Takuji Okamura[1]
Manabu Tomisaka[2], Hitoshi Yonemura[2]
Masataka Hoshino[2], and Kenji Takahashi[2]
* E-mail: kkondo@cc.okayama-u.ac.jp
[1] Dept.of Appl. Chem., Engineering, Okayama University
3-1-1, Tsushima-naka, Okayama, 700-0082, Japan

[2] Electronic System Integration Technology Research Department, Association of Super-Advanced Electronic Technologies (ASET)
1-6, Sengen 2-chome, Tsukuba, Ibaraki 305-0047, Japan

Recently three-dimensional (3D) packaging technology has attracted much attention because of the requirement of high density, high performance and lower energy consumption for the electronic devices. Thinned silicon chips down to 50μm in thickness are stacked and shortest interconnection among them is offered by through chip copper plugs, and signal delay can be reduced to the lowest level (Fig.1) [1-3].

Sizes of the through plugs are in the range of 50μm ~ 100μm in length and 5μm~20μm in diameter, which are 100 times larger in length than that of the Damascence, hence the mechanism of copper electrodeposition through chip plug might be different from that of Damascence copper process used for LSI interconnection [4-10].

In this presentation, factors to influence the bottom-up filling in vias are discussed, including the additives' concentration, current density, via patterns and mass transfer. Under a proper electrodeposition condition, vias with depth in 50 ~ 70μm and square side in 10μm, 8μm, 6μm used for through chip copper plug were fully filled with void free (Fig. 2).

Acknowledgments

The work was supported by NEDO as a part of the project of "Research and Development of Ultra High-density Electronics System Integration Technology".

References

[1] M. Koyanagi, T.Nakamura, K.W.Lee, Y.Igarashi, T.Mizukusa, Y.Yamada, T.Morooka, and H.Kurino, Advanced Metalization Conference, Montreal ,20 (2001).
[2] M.Tomisaka, H. Yonemura, M.Hoshino, and K. Takahashi, Solid State Devices and Materials, Tokyo,40 (2001).
[3] K. Takahashi, The 2ed Annual Meeting on Electronic SI Technologies, ,Tokyo, 27(2001).
[4] P.C. Andricacos, C. Uzoh, J.O. Dukovic, J. Horkans, H. Deligianni, IBM J. Res. Develop. 42, 567 (1998).
[5] T.P. Moffat, J.E. Bonevich, W. H. Huber, A. Stanishevsky, D.R. Kelly, G.R.Stafford, and D. Josell, J. Electrochem. Soc. 147, 4524 (2000).
[6] P. Taephaisitphongse, Y. Cao, A. C. West, J. Elecotrochem. Soc.148, C492 (2001).
[7] K.Kondo, T.Okamura and Z.Tanaka,'Effect of via opening width on Copper via filling electrodeposition', MES2001, Osaka, 95 (2001).
[8] K. Kondo, K. Hayashi, Z. Tanaka and Yamakawa, JIEP 3, 607(2000).
[9] K. Kondo and N. Yamakawa, ISTC2001, Shanghai , 532 (2001).
[10] K. Kondo, ECS Abstract 764, San Francisco, (2001).

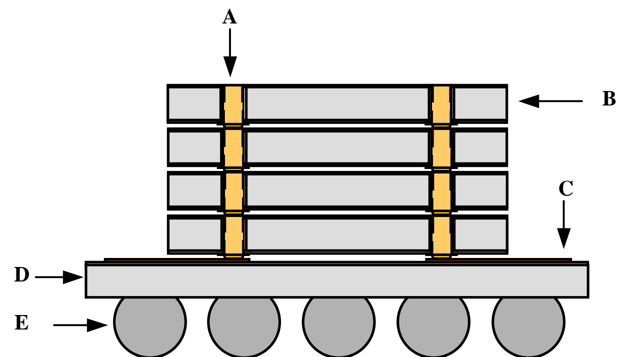

Fig. 1 Schematic illustration of chip stacking for 3D packaging. (A) Through chip Cu plug (B) Thinning chip (C) Pad (D) Interposer (E) Solder ball.

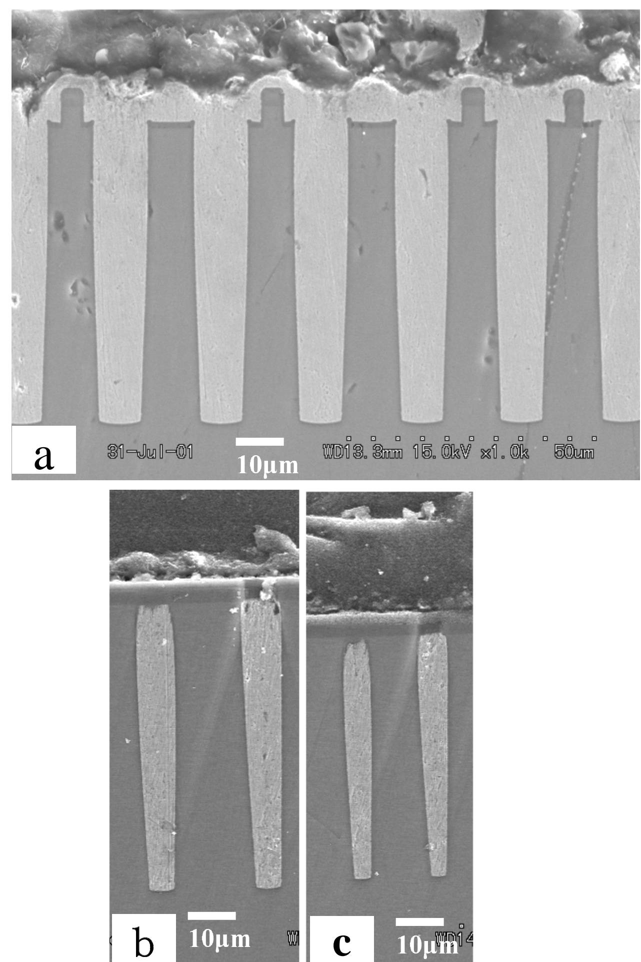

Fig. 2 SEM of the cross section of completely filled vias used for through chip plugs on silicon chip with depth of 50 ~ 70μm and square of (a) 10μm (b) 8μm (c) 6μm.