Realizing the Future for the Semiconductor Industry - Meeting the Challenges of Process, Design and Business

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The semiconductor industry has evolved into one of the critical foundations for the global economy. Not only has it reached a revenue level well in excess of $150B per year, its continued long term growth at an average rate of 15% will quickly propel it into one of the largest value add factors of many national economies. In addition, ever improving cost, performance and scale of integration allow integrated circuits to continuously enable new products, both business and consumer. The productivity improvements brought about by data and wireless communications, personal computers and the Internet have become a major factor in the growth of both national and global economies.

However, the industry is not without challenges, and these challenges must be addressed if we are to continue on our historic growth track. The challenges include process and material issues, (especially as we move into design dimensions where our historic technologies will no longer work), managing the design complexity of very large integrated circuits, and a variety of business issues.

On of the most significant technical challenges is to extend optical lithography deep into the sub-wavelength regime at the 70nm design node, and to do so cost effectively, which means that the mask technology and cycle times will have to be significantly improved. Following this extension we will need to move to a next generation technology, such as EUV, for design rules below 70nm, and this will represent a major change.

At 70nm and below, interconnect delays using standard materials become prohibitive and very low-k dielectrics will be needed, most likely consisting of porous organic films. The integration of such films, with their poor thermo-mechanical properties will be a major challenge. To help mitigate this problem, we will need the careful integration of interconnection between on chip and off chip (packaging).

Planar CMOS technology, the bedrock of semiconductor production, will also begin to see problems at 70nm. A series of advances will be needed to retain our improvements in speed power product, including high-k gate dielectrics to reduce leakage currents, the introduction of metal gates to avoid poly-silicon depletion effects, and the use of ultra-shallow junctions and non-equilibrium annealing techniques to avoid transient enhanced diffusion. In addition, the industry will use a variety of material advances to handle higher frequencies and lower power devices, including SiGe, strained silicon, SOI and GaAs on silicon epitaxy. Finally, at around 20nm we will need to reconsider the whole concept of planar CMOS devices as the physics becomes increasingly difficult.

Combined with the technology challenges, are a significant array of design and test issues that must also be addressed. The massive scales of integration will mandate design at much higher levels of abstraction, including the significant reuse of major blocks of design code. Assuring interface standards, testability and quality of design will be a particular challenge that is not easily solved. At the same time, the more specific challenges at a local level in the design process - for example, maintaining signal and clock integrity on very fast circuits, will require much better layout/timing tools than presently available, nor will human intervention be as easy as the circuits grow in size and speed. Design for reasonable power dissipation and current management will also have to manage the trade off between lower voltages to reduce power dissipation and higher current spikes as clock speeds increase.

Finally, the industry is not without business challenges. Probably the most visible of these is the constant imbalance of supply and demand, causing major cyclicality swings. Although the revenue trends are upwards, the downturns, when they happen can be very difficult to manage. The onset of 300mm fabs, with their higher cost and productivity will only serve to exacerbate these swings in the future and, combined with the intrinsic cyclicality of the industry, may lead to significant consolidation in manufacturing. Environmental, safety and health issues must also be addressed. The rapid growth of the industry mandates better water and energy conservation to assure sustainable growth. At the same time, the very rapid process/material developments require careful consideration of the environmental impact of these advances.

However, the industry is aware of all of these challenges and has marshaled resources to attack them. This paper will review the challenges and the proposed solutions and will also discuss the role of consortia is helping to resolve them.