ESTABLISHMENT OF A DEVICE PROCESS PLATFORM FOR REALIZING A LEADING-EDGE SYSTEM-ON-A-CHIP

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ABSTRACT

It is well recognized that the role of semiconductor technology, especially SoC (System-on-a-Chip) will be increasingly significant in an IT (Information Technology) society. A new project targeting for establishing the platforms for developing a leading-edge SoC with 100 – 70 nm technology started in April, 2001, in Japan.

This report describes the development of device/process platform for SoC, as a part of the above project. Three key process modules, that is, 1) lithography and mask, 2) a transistor which employs a high κ dielectric, and 3) a multi-layer interconnect with Cu and low κ inter-layer dielectric, will be developed.

One of the most tough subjects is the selection of the best high κ material for the gate dielectric, and integrate it into the CMOS process. The same situation is true for the low κ material for inter-layer dielectric of multi-layer interconnect.

The paper will cover the development strategy & plan, examples of achievements up to now, and global collaboration.