MIRAI Project

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The MIRAI project is authorized by the New Energy and Industrial Technology Organization (NEDO) under a program funded by the Ministry of Economy, International Trade and Industry (METI) of Japan. The MIRAI project is conducted by a virtual organization of researchers from the Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST) and the Association of Super-Advanced Electronics Technologies (ASET) in cooperation with academia under Project Leader Masataka Hirose, Director-General of ASRC, AIST. The main site for research is the Tsukuba Super Cleanroom, now under construction and scheduled for completion in March 2002. The Project R&D themes focus on state-of-the-art semiconductor technology for realizing the 70-50nm node and beyond, which cover the five key areas such as: (1) Gate Stack Technology with High-k Materials, (2) Interconnect Module Technology with Low-k Materials, (3) New Transistor Structures and Measurement/ Analysis Technology, (4) Lithography and Mask Related Metrology and Inspection, and (5) New Circuits and System Technology. The five R&D groups have been extensively working in Tsukuba since August, 2001. The first term of the Project is 2001-2003, and the second 2004-2007.
MIRAI Project Leader is fully responsible for the R&D activities of the five groups. Each of the groups is led by the distinguished specialist with excellent achievements and clear vision for research.

In high-k gate stack technology for CMOS, where issues to be overcome are tightly connected to fundamental physics of devices and materials, MIRAI believes that the science based research over phenomenological understandings should be conducted for developing the process module. Employing the high-k gate dielectric materials for CMOS needs to simultaneously realize the performance improvement and the whole device integration by totally satisfying the scaling scenario. It should be carefully examined whether various technical issues are due to the intrinsic nature of the high-k material or due to the immaturity of related technologies for advanced devices.

Ultra-low-k interlayer dielectric films and Cu interconnect technologies are now being developed by scientific and systematic approaches in conjunction with material analysis techniques. High-performance Cu/low-k interconnect module technologies will be demonstrated by the use of practical 300 mm process tools. Goals of this project are to develop new interlayer dielectric materials which have sufficient mechanical properties against chemical mechanical polishing and ultra-low dielectric constant less than 1.5.

Developing new transistor structures by implementing new materials and channel engineering methodology is required for SoC beyond the 50nm technology node. MIRAI focuses on strained-Si channel MOSFETs and related technology developments including ultra shallow junction formation.

Advances in metrology and inspection technologies are essential to the reduction of feature size and introduction of new materials and processes for future technology generation. The metrology and inspection topics selected in the MIRAI Project are mask inspection and minimum feature size measurements, related to lithography for the 50-nm technology node and beyond and to micro-particle identification.

Yield enhancement in the high-end digital LSIs is one of main concerns, while in analog LSIs circuitry for offset reduction in yield is often needed despite increased chip size and power consumption. One of promising approaches to solving the deterioration of yield is to incorporate adjustable circuitry for the parameters that influence yields and to adjust these with genetic algorithms. Adjustable circuit structures and adjusting algorithms can be applied not only to digital LSIs but analog LSIs .