Low Voltage Gate Dielectric Reliability

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Gate dielectric reliability has been an important concern for successive generations of CMOS. In particular, extrapolation from the higher voltages used in testing to the operating voltage has been an important consideration. Experimental and simulation work on ultra-thin oxides has shown that NMOS devices can be safely operated at voltages higher than was previously thought[1,2], and these results have been confirmed by several other groups.[3] However, PMOS acceleration factors remain in question due to minority ionization and the damage that could occur from cold-hole tunneling. Because of minority ionization, we would expect a lower voltage acceleration for PMOS than NMOS in the 3-5V range.[2] Below ~2.5V, for thin oxides, where cold-hole tunneling is a significant portion of the current, further measurements were required. Since it is time-consuming to perform low-voltage TDDB measurements, we used stress-induced leakage current to gain information about the voltage acceleration for PMOS devices. From these measurements (fig. 1), we have obtained a voltage acceleration factor which is significantly more optimistic than that obtained from higher voltage measurements, and convincingly demonstrates a non-linear voltage acceleration for PMOS. This indicates that the main damage continues to come from holes produced by energetic electrons rather than from cold holes (see fig. 2). Given these voltage acceleration factors, PMOS devices should be reliable for many applications. However, if the operating voltage is increased so that PMOS devices cannot meet conventional reliability criteria, additional margin may be obtained by considering soft breakdown.[1,4]

In a close interaction between experiment and simulation, we have found the relationship between soft breakdown and transistor geometry, dielectric thickness, stress voltage, and stress type leading to a broad-based understanding and predictive capability. We show that the main controlling parameter for soft breakdown is voltage and that even breakdowns in small devices or those occurring near the drain can be soft if the stress voltage or compliance is low. As shown in fig. 3a, when we use a position detection technique developed by Degraeve et al.[4], breakdowns occurring at the drain-end of the transistor have the largest effect on I_{off}, but even when the breakdown spot is located in the gate-drain overlap region, the transistor is still functional. The threshold voltage (fig. 3b) shows no dependence on breakdown position, but a dependence on the stress time was observed (not shown). Therefore, we see no indication that circuits will be disrupted by a few soft breakdowns. However, it remains to be seen how much additional reliability margin can be added by understanding soft breakdown.

Oxide breakdown has been a concern for digital circuits, but in analog circuits where such concerns as threshold voltage matching arise, other types of degradatoin have become important as well. One measurement which particularly aims to track parameters such as threshold voltage as a function of stress-time is the bias-temperature stress measurement. Standard bias-temperature stress models with a $t^{1/2}$ dependence at long times indicate that it could be difficult to ensure the reliability of PMOS devices with ultra-thin oxides. Extensive measurements are necessary to understand the phenomenon.

In conclusion, our results provide assurance that PMOS voltage acceleration increases at lower voltage although not at the same rate as NMOS does. We also show that breakdown will be soft for the voltages and geometries used in future technologies.

1 B. E. Weir et al. *Semicond. Sci. Tech.* **15** p.455, 2000.
2 M. A. Alam et al. IRPS 2000, p.21 and refs. therein.
3 E. Y. Wu et al. IEDM 2000, p.541.
4 R. Degraeve et al. IRPS 2001, p.360.

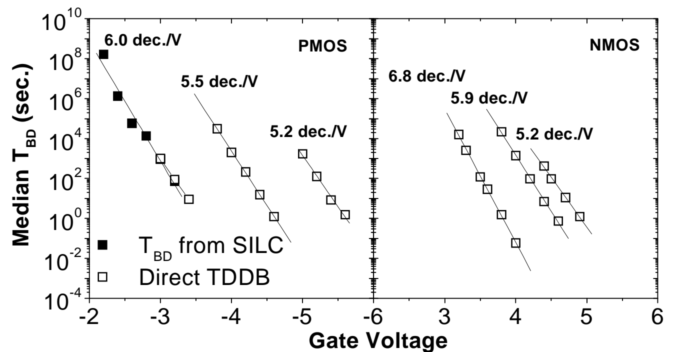

Fig. 1: Time to breakdown vs. Stress Voltage for n- and p-MOSFETs. Soft breakdown was measured on $2.5x10^{-8}$ cm^2 devices at room temperature. The voltage acceleration factors noted are from a least squares fit of all of the voltage points for a given thickness.

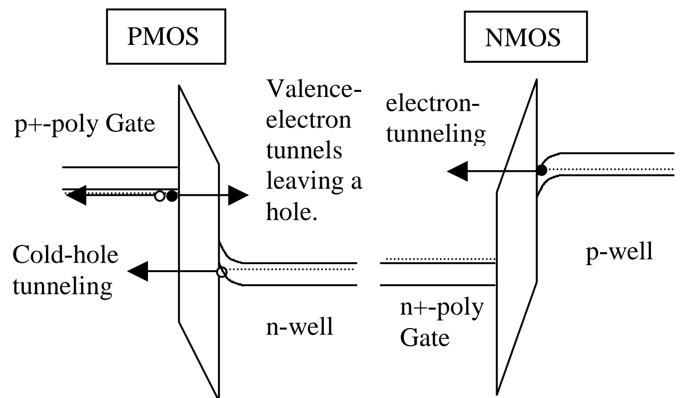

Fig. 2: Band-diagram for PMOS and NMOS. Both the effect of tunneling electrons from the valence band and cold-hole tunneling must be considered for the PMOS case, while the NMOS case is dominated by conduction-band electron tunneling.

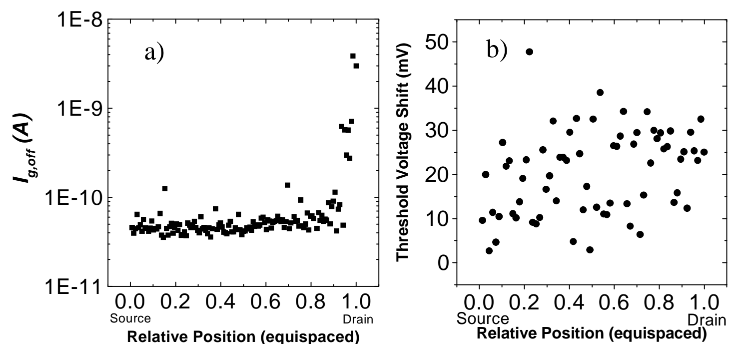

Fig. 3: a) Gate-current component of I_{off} vs. breakdown position.[4] b) Threshold voltage shift shows no correlation to breakdown spot position within the 0.16μm transistor. 1.7nm oxide devices were stressed at 3.8V with 20μA compliance.