Electric stress-induced degradation of thin oxide layers and its impact on device reliability

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This paper presents an overview of how electrical stress-induced degradation can be a reliability problem in microelectronic devices. Depending on the application a different amount of oxide degradation can be tolerated, and this determines the limiting thickness down to which the oxide can be scaled.

OXIDE DEGRADATION PROCESS

We can think of thin oxide layer degradation by electrical stress as the continuous generation of point defects in the layer. The exact trap generation mechanism is still under discussion. Basically, two ideas have been proposed in literature: one assumes direct involvement of the electric field (electrochemical model) [1], the second proposes a current-driven mechanism with the defect-generating species being either holes [2] or hydrogen [3]. Several recently performed dedicated experiments favor the current driven model [4] but the nature of the degrading species is still not certain. In this paper, it is not our intention to describe in detail the microscopic structure of the oxide defects, neither to discuss their exact generation mechanism. It suffices to state that 1) the traps are mostly neutral, 2) they can trap electrons and 3) they are generated at random places in the bulk of the layer. A statistical treatment of the random generation pattern with the introduction of electrical trap-trap interaction is sufficient to understand and predict many oxide reliability phenomena.

STRESS-INDUCED LEAKAGE CURRENT

The electron traps generated during the stress create local energy levels in the bandgap of the oxide that facilitate tunneling of carriers from cathode to anode. This gives rise to the Stress-Induced Leakage Current (SILC) which can be particularly observed at low oxide field in the normal operation range of many devices. SILC is a reliability concern in any device where very low leakage current is mandatory for a proper operation. Floating gate memories are a typical example. The memory function is jeopardized as soon as the charge stored on the floating gate can leave it unintentionally.

The largest component in the SILC is caused by trap-assisted tunneling through single traps. But when the trap density is sufficiently high, a configuration of two traps can appear through which the electrons tunnel more efficiently from cathode to anode. This gives rise to the ‘anomalous’ leakage current. This anomalous SILC-component is a severe reliability limitation for the thickness scaling of non-volatile memory tunnel oxides, limiting the maximum thickness to about 7-8 nm.

The anomalous SILC is also the cause of small pre-breakdown current steps observed during time-to-breakdown measurements on small area devices [5]. These jumps complicate the detection of the final oxide breakdown on test structures. Only detection methods based on the increase of the gate current noise can correctly distinguish between a pre-breakdown current increase and a real oxide breakdown [6].

SOFT AND HARD BREAKDOWN

When a conduction path of traps is formed in the oxide connecting the cathode with the anode interface, the oxide layer breaks down. Breakdown can be viewed as an extreme case of anomalous SILC, where the local current through the path exceeds a critical value. Two breakdown modes have been observed experimentally. In case of *soft* breakdown the current flow through the breakdown path is insufficient to cause thermal runaway, contrary to the case of *hard* breakdown.

Although hard breakdown is very destructive for the insulating properties of the thin oxide layer, it does not necessarily cause a circuit to fail. Indeed, when the circuit failure criterion is defined based on its functionality, even a hard oxide breakdown is not necessarily coinciding with failure. We have demonstrated this by means of a simple ring oscillator circuit, which keeps oscillating even after several of its composing transistors underwent hard breakdown [7]. In all cases, however, where an increase of the leakage current cannot be tolerated – low power battery application e.g. – hard breakdown can be a problem.

In recent literature, experimental evidence together with detailed simulations indicate that in the normal operation voltage range of many devices, the occurrence of hard breakdown is strongly suppressed and only soft breakdown is triggered [8]. Since soft breakdown causes only a moderate leakage current increase, it is far less destructive and will in many cases not cause circuit failure. With these considerations in mind, the oxide thickness scaling in CMOS technologies is not limited by reliability, but by other factors as e.g. the direct tunnel current.

CONCLUSION

In conclusion, most reliability issues can be understood if oxide degradation is viewed as the continuous creation of electron traps, generating single and multiple trap SILC and causing finally oxide breakdown. The amount of degradation that can be tolerated strongly depends on the application.

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