CHARACTERIZATION OF THE MECHANICAL STRESS INDUCED DURING SILICIDATION IN SUB-0.25μM MOS TECHNOLOGIES

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The objective set forward for the present work was to investigate the influence of the mechanical stress, induced during the silicidation, and combined with the isolation stress, on the device characteristics in sub-0.25μm MOS technologies.

Mechanical stress analysis in silicide films

During the silicidation reaction, two sources of silicide stress can be observed: an intrinsic compressive stress, due to the volume changes during the silicide formation and a tensile thermal stress, due to the difference in thermal expansion coefficient between the silicide and the Si-substrate. The intrinsic compressive stress induced during the Ti-silicidation is higher than the intrinsic stress induced during the Co-silicidation. After formation of $TiSi_2$ and $CoSi_2$ at elevated temperature, a thermal stress builds up in both silicide films. The thermal stress is tensile because the thermal expansion coefficient of $TiSi_2$ and $CoSi_2$ is higher than the thermal expansion coefficient of silicon. The residual built-in stress at room temperature is 2.1GPa for $TiSi_2$ and 1.1GPa for $CoSi_2$. In situ stress measurements during the Ni-silicidation have shown that the built-in stress at room temperature is 720MPa for NiSi.

Mechanical stress analysis in and around narrow silicide lines

It is investigated how the residual built-in stress in the silicide changes for submicrometer silicide line patterns and which effect the silicide stress has on the stress in the Si-substrate. The stress in the Si-substrate can be attributed to the superposition of the stress fields of all line edges. When scaling down the line pitch, the stress fields at the edges of neighboring lines start to interfere, resulting in a higher stress in the Si-substrate at the line interface. The stress is determined by using experimental (μRS and CBED) and numerical (FEM) stress measurement techniques. In case of a silicide/oxide line pattern, the lateral stress component is tensile underneath the oxide and compressive underneath the silicide. Because of the transition from the tensile to the compressive stress, the most critical stress location occurs at the line edge. Both μRS and FEM show an increase of the local stress in the Si-substrate underneath the lines when reducing the line pitch and when increasing the silicide thickness. $TiSi_2$ induces almost twice as much thermal stress in the Si-substrate as $CoSi_2$ because of the difference in material properties between both silicides. NiSi induces almost no stress in the Si-substrate. The stress in the Si-substrate is the highest at the line interface. At a silicon depth below 1μm underneath the line interface, the influence of the silicide and oxide stress is no longer observed.

Silicide stress induced defects in the silicon lattice

When scaling down the device dimensions and increasing the pattern density, the local mechanical stress in the silicon substrate induced during the Ti- and Co/Ti silicidation increases. When the shear stress exceeds the critical yield stress of silicon at elevated temperature, 60° dislocations are generated in the Si-substrate underneath the silicide lines on the (-111) and (1-11) glide planes along the [110] oriented line edge. These dislocations nucleate at the line edges. When reducing the line width, the 60° dislocations multiply following a process of multiple cross glide. $TiSi_2$ induces a higher stress than $CoSi_2$, resulting in a higher number of dislocations for the same width/thickness ratio.

Influence of the silicide pattern density on the electron / hole mobility in the transistor channel

The effect of a mechanical stress on the electron and hole mobility in the NMOS and PMOS transistor channel has been investigated. The mechanical stress in the transistor channel is varied by using a transistor structure with variable S/D spacing and S/D width. When reducing the S/D spacing or increasing the silicide thickness, an increasing biaxial tensile stress is generated in the transistor channel and an increasing compressive stress normal to the Si plane. For the electron mobility, a biaxial tensile stress in the (001)Si plane leads to a redistribution of the electrons over the six energy valleys of the valence band. The two lower energy valleys with a lower effective mass, hence a higher overall mobility, are more populated with electrons than the four higher energy valleys with a higher effective mass. This means that a tensile biaxial stress in the (001)Si plane enhances the overall electron mobility. For the hole mobility, a tensile biaxial stress splits the valence bands in such a way that the light holes are favorably filled up. Moreover, the effective mass of the light and heavy holes is also getting smaller for increasing stress. This leads to an overall hole mobility enhancement. A compressive biaxial stress splits the valence band in such a way that the heavy holes are favorably filled up. For small stress fields, a hole mobility reduction is observed.